Tiger Lake UP3 UP4 H35 UP3 Refresh Platform

Schematic Checklist

Revision 2.2

November 2020

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Revision History

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| 607872 | 0.7 | * Initial release | April 2019 |
| 0.9 | * Updated SPI section and added strap details * Updated GPIO section * Updated Platform Clocks: PCIe CLKOUT and SRCCLKREQ port numbers * Removed SPI1 section | April 2019 |
| 1.0 | * Removed RCOMP [1] and RCOMP [2] from all memory topology. * Updated the termination resistor value SPI0 1/2/3 load topology and EC Isolation FET Flash Sharing topology. * Updated UART Pin Name * Updated PCH PCIe\*: UP4 port numbers * UART pin name changed from UART[1:0] to UART[2:0] | October 2019 |
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| 607872 | 2.2 | * Added note under table in Section 1.6 CSI and Imaging Clock * Added Table 3 TCP Disabling and Termination Guidelines for USB Type C interface * Added Table 8 Disabling and Termination Guidelines for Digital Display interface | November 2020 |

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# Schematic Checklists

## System Memory

### Tiger Lake UP3 DDR4 SoDIMM Checklist

|  |  |  |
| --- | --- | --- |
| **Pin Name** | **Schematic Notes** | **Notes** |
| DDR0\_CLK\_P[1:0]/ DDR1\_CLK\_P[1:0] | Connect to DIMM[0] connector CK[1:0]P pins | 1 |
| DDR0\_CLK\_N[1:0]/ DDR1\_CLK\_N[1:0] | Connect to DIMM[0] connector CK[1:0]N pins | 1 |
| DDR0\_CS#[1:0]/ DDR1\_CS#[1:0] | Connect to DIMM[0] connector CS[1:0]\_N pins |  |
| DDR0\_CKE[1:0]/ DDR1\_CKE[1:0] | Connect to DIMM[0] connector CKE[1:0] pins |  |
| DDR0\_ODT[1:0]/ DDR1\_ODT[1:0] | Connect to DIMM[0] connector ODT[1:0] pins |  |
| DDR0\_MA[16:0]/ DDR1\_MA[16:0] | Connect to DIMM[0] connector A[16:0] pins |  |
| DDR0\_BG[1:0]/ DDR1\_BG[1:0] | Connect to DIMM[0] connector BG[1:0] pins |  |
| DDR0\_BA[1:0]/ DDR1\_BA[1:0] | Connect to DIMM[0] connector BA[1:0] pins |  |
| DDR0\_ACT#/ | Connect to DIMM[0] connector pin |  |
| DDR0\_PAR/ DDR1\_PAR | Connect to DIMM[0] connector pin |  |
| DDR0\_ALERT#/ DDR1\_ALERT# | Connect to DIMM[0] connector pins |  |
| DDR0\_DQ[7:0][7:0] | Connect to ch0 DIMM[0] connector DQ[63:0] pins | 2, 3 |
| DDR1\_DQ[7:0][7:0] | Connect to ch1 DIMM[0] connector DQ[63:0] pins | 2, 3 |
| DDR0\_DQSP[7:0]/ DDR0\_DQSN[7:0] | Connect to DIMM[0] connector DQSP[7:0]/DQSN[7:0] pins | 3, 4 |
| DDR1\_DQSP[7:0]/ DDR1\_DQSN[7:0] | Connect to DIMM[1] connector DQSP[7:0]/DQSN[7:0] pins | 3, 4 |
| DM[7:0] | Tie DIMM connector DM[7:0] pins directly to VDDQ |  |
| DDR0\_VREF\_CA | Connect to VREF\_CA of Channel A (DDR0\_XXX signals) DIMMs. Refer to System Memory Interface Design Guideline Chapter in Platform Design Guide. |  |
| DDR1\_VREF\_CA | Connect to VREF\_CA of Channel B (DDR1\_XXX signals) DIMMs. Refer to System Memory Interface Design in PDG. |  |
| DRAM\_RST# | Refer to System Memory Interface Design Guidelines Chapter in Platform Design Guide. | 5 |
| DDR\_RCOMP | Refer to System Memory Interface Design Guidelines Chapter in Platform Design Guide. |  |

* 1. CKP and CKN differential signal swapping within a pair is not allowed. Also, differential clock pair to clock pair swapping within a channel is not allowed.
  2. DQ Bit swapping is allowed within the same byte
  3. Byte Swapping is allowed within the same channel
  4. DQSP and DQSN differential signal swapping within a pair is not allowed.
  5. Capacitor C1 is a defensive design and should be NO STUFF by default.

### Tiger Lake UP3 DDR4 x16 Memory Down Checklist

|  |  |  |
| --- | --- | --- |
| **Pin Name** | **Schematics Notes** | **Notes** |
| DDR0\_CLK\_P[0]/ DDR0\_CLK\_N[0] | Connect to ch0 DRAMs CK\_t/CK\_c balls Connect to Rtt | 1 |
| DDR1\_CLK\_P[0]/ DDR1\_CLK\_N[0] | Connect to ch1 DRAMs CK\_t/CK\_c balls Connect to Rtt | 1 |
| DDR0\_CLK\_P[1]/ DDR0\_CLK\_N[1] | Not connected |  |
| DDR1\_CLK\_P[1]/ DDR1\_CLK\_N[1] | Not connected |  |
| DDR0\_CS#[0]/ DDR1\_CS#[0] | Connect to DRAMs CS\_n balls Connect to Rtt |  |
| DDR0\_CS#[1]/ DDR1\_CS#[1] | Not connected |  |
| DDR0\_CKE[0]/ DDR1\_CKE[0] | Connect to DRAMs CKE balls Connect to Rtt |  |
| DDR0\_CKE[1]/ DDR1\_CKE[1] | Not connected |  |
| DDR0\_ODT[0] / DDR1\_ODT[0] | Connect to DRAMs ODT balls Connect to Rtt |  |
| DDR0\_ODT[1] / DDR1\_ODT[1] | Not connected |  |
| DDR0\_MA[16:0]/ DDR1\_MA[16:0] | Connect to DRAMs A[16:0] balls Connect to Rtt |  |
| DDR0\_BG[1:0]/ DDR1\_BG[1:0] | For SDP only connected to DRAMs BG[0] balls  ,BG[1] not connected  For DDP only connected to BG [1:0] balls Connect to Rtt |  |
| DDR0\_BA[1:0]/ DDR1\_BA[1:0] | Connect to DRAMs BA[1:0] balls Connect to Rtt |  |
| DDR0\_ACT#/ DDR1\_ACT# | Connect to DRAMs ACT\_n balls Connect to Rtt |  |
| DDR0\_PAR/ DDR1\_PAR | Connect to DRAMs PAR balls Connect to Rtt |  |
| DDR0\_ALERT#/ DDR1\_ALERT# | Should be left NC at SOC  Alert should be daisy chained to DRAMs and connected to VDDQ at the end through a 50 ohm resistor |  |
| DDR0\_DQ0[7:0]/ DDR0\_DQ1[7:0] | Connect to ch0 DRAM0 DQ[15:0] balls | 2, 3 |
| DDR0\_DQ2[7:0]/ DDR0\_DQ3[7:0] | Connect to ch0 DRAM1 DQ[15:0] balls | 2, 3 |
| DDR0\_DQ4[7:0]/ DDR0\_DQ5[7:0] | Connect to ch0 DRAM2 DQ[15:0] balls | 2, 3 |
| DDR0\_DQ6[7:0]/ DDR0\_DQ7[7:0] | Connect to ch0 DRAM3 DQ[15:0] balls | 2, 3 |
| DDR1\_DQ0[7:0]/ DDR1\_DQ1[7:0] | Connect to ch1 DRAM0 DQ[15:0] balls | 2, 3 |
| DDR1\_DQ2[7:0]/ DDR1\_DQ3[7:0] | Connect to ch1 DRAM1 DQ[15:0] balls | 2, 3 |
| DDR1\_DQ4[7:0]/ DDR1\_DQ5[7:0] | Connect to ch1 DRAM2 DQ[15:0] balls | 2, 3 |
| DDR1\_DQ6[7:0]/ DDR1\_DQ7[7:0] | Connect to ch1 DRAM3 DQ[15:0] balls | 2, 3 |
| DDR0\_DQSP[0]/ DDR0\_DQSN[0] | Connect to ch0 DRAM0 UDQS\_C/T balls | 3, 4 |
| DDR0\_DQSP[1]/ DDR0\_DQSN[1] | Connect to ch0 DRAM0 DQS\_C/T balls | 3, 4 |
| DDR0\_DQSP[2]/ DDR0\_DQSN[2] | Connect to ch0 DRAM1 UDQS\_C/T balls | 3, 4 |
| DDR0\_DQSP[3]/ DDR0\_DQSN[3] | Connect to ch0 DRAM1 DQS\_C/T balls | 3, 4 |
| DDR0\_DQSP[4]/ DDR0\_DQSN[4] | Connect to ch0 DRAM2 UDQS\_C/T balls | 3, 4 |
| DDR0\_DQSP[5]/ DDR0\_DQSN[5] | Connect to ch0 DRAM2 DQS\_C/T balls | 3, 4 |
| DDR0\_DQSP[6]/ DDR0\_DQSN[6] | Connect to ch0 DRAM3 UDQS\_C/T balls | 3, 4 |
| DDR0\_DQSP[7]/ DDR0\_DQSN[7] | Connect to ch0 DRAM3 DQS\_C/T balls | 3, 4 |
| DDR1\_DQSP[0]/ DDR1\_DQSN[0] | Connect to ch1 DRAM0 UDQS\_C/T balls | 3, 4 |
| DDR1\_DQSP[1]/ DDR1\_DQSN[1] | Connect to ch1 DRAM0 DQS\_C/T balls | 3, 4 |
| DDR1\_DQSP[2]/ DDR1\_DQSN[2] | Connect to ch1 DRAM1 UDQS\_C/T balls | 3, 4 |
| DDR1\_DQSP[3]/ DDR1\_DQSN[3] | Connect to ch1 DRAM1 DQS\_C/T balls | 3, 4 |
| DDR1\_DQSP[4]/ DDR1\_DQSN[4] | Connect to ch1 DRAM2 UDQS\_C/T balls | 3, 4 |
| DDR1\_DQSP[5]/ DDR1\_DQSN[5] | Connect to ch1 DRAM2 DQS\_C/T balls | 3, 4 |
| DDR1\_DQSP[6]/ DDR1\_DQSN[6] | Connect to ch1 DRAM3 UDQS\_C/T balls | 3, 4 |
| DDR1\_DQSP[7]/ DDR1\_DQSN[7] | Connect to ch1 DRAM3 DQS\_C/T balls | 3, 4 |
| DMU, DML | Tie all DRAMs DMU and DML balls directly to VDDQ. |  |
| DDR0\_VREF\_CA | Connect to VREF\_CA of Channel A (DDR0\_XXX) |  |
| DDR1\_VREF\_CA | Connect to VREF\_CA of Channel B (DDR1\_XXX) |  |
| DRAM\_RST# | Refer to System Memory Interface Design Guideline |  |
| DDR\_RCOMP | Refer to System Memory Interface Design Guideline |  |

* 1. CKP and CKN differential signal swapping within a pair is not allowed.
  2. DQ Bit Swapping is allowed within the same byte.
  3. Byte Swapping is allowed within the same channel.
  4. DQSP and DQSN differential signal swapping within a pair is not allowed.

### Tiger Lake UP3 DDR4 x8 Memory Down Checklist

|  |  |  |
| --- | --- | --- |
| **Pin Name** | **Schematics Notes** | **Notes** |
| DDR0\_CLK\_P[0]/ DDR0\_CLK\_N[0] | Connect to ch0 DRAMs CK\_t/CK\_c balls Connect to Rtt | 1 |
| DDR1\_CLK\_P[0]/ DDR1\_CLK\_N[0] | Connect to ch1 DRAMs CK\_t/CK\_c balls Connect to Rtt | 1 |
| DDR0\_CLK\_P[1]/ DDR0\_CLK\_N[1] | Not connected |  |
| DDR1\_CLK\_P[1]/ DDR1\_CLK\_N[1] | Not connected |  |
| DDR0\_CS#[0]/ DDR1\_CS#[0] | Connect to DRAMs CS\_n balls Connect to Rtt |  |
| DDR0\_CS#[1]/ DDR1\_CS#[1] | Not connected |  |
| DDR0\_CKE[0]/ DDR1\_CKE[0] | Connect to DRAMs CKE balls Connect to Rtt |  |
| DDR0\_CKE[1]/ DDR1\_CKE[1] | Not connected |  |
| DDR0\_ODT[0] / DDR1\_ODT[0] | Connect to DRAMs ODT balls Connect to Rtt |  |
| DDR0\_ODT[1] / DDR1\_ODT[1] | Not connected |  |
| DDR0\_MA[16:0]/ DDR1\_MA[16:0] | Connect to DRAMs A[16:0] balls. Connect to Rtt |  |
| DDR0\_BG[1:0]/ DDR1\_BG[1:0] | Connect to DIMMs BG[1:0] balls Connect to Rtt |  |
| DDR0\_BA[1:0]/ DDR1\_BA[1:0] | Connect to DRAMs BA[1:0] balls Connect to Rtt |  |
| DDR0\_ACT#/ DDR1\_ACT# | Connect to DRAMs ACT\_n balls Connect to Rtt |  |
| DDR0\_PAR/ DDR1\_PAR | Connect to DRAMs PAR balls Connect to Rtt |  |
| DDR0\_ALERT#/ DDR1\_ALERT# | Should be left NC at SOC  Alert should be daisy chained to DRAMs and connected to VDDQ at the end through a 50 ohm resistor |  |
| DDR0\_DQ0[7:0] | Connect to ch0 DRAM0 DQ[7:0] balls | 2, 3 |
| DDR0\_DQ1[7:0] | Connect to ch0 DRAM1 DQ[7:0] balls | 2, 3 |
| DDR0\_DQ2[7:0] | Connect to ch0 DRAM2 DQ[7:0] balls | 2, 3 |
| DDR0\_DQ3[7:0] | Connect to ch0 DRAM3 DQ[7:0] balls | 2, 3 |
| DDR0\_DQ4[7:0] | Connect to ch0 DRAM4 DQ[7:0] balls | 2, 3 |
| DDR0\_DQ5[7:0] | Connect to ch0 DRAM5 DQ[7:0] balls | 2, 3 |
| DDR0\_DQ6[7:0] | Connect to ch0 DRAM6 DQ[7:0] balls | 2, 3 |
| DDR0\_DQ7[7:0] | Connect to ch0 DRAM7 DQ[7:0] balls | 2, 3 |
| DDR1\_DQ0[7:0] | Connect to ch1 DRAM0 DQ[7:0] balls | 2, 3 |
| DDR1\_DQ1[7:0] | Connect to ch1 DRAM1 DQ[7:0] balls | 2, 3 |
| DDR1\_DQ2[7:0] | Connect to ch1 DRAM2 DQ[7:0] balls | 2, 3 |
| DDR1\_DQ3[7:0] | Connect to ch1 DRAM3 DQ[7:0] balls | 2, 3 |
| DDR1\_DQ4[7:0] | Connect to ch1 DRAM4 DQ[7:0] balls | 2, 3 |
| DDR1\_DQ5[7:0] | Connect to ch1 DRAM5 DQ[7:0] balls | 2, 3 |
| DDR1\_DQ6[7:0] | Connect to ch1 DRAM6 DQ[7:0] balls | 2, 3 |
| DDR1\_DQ7[7:0] | Connect to ch1 DRAM7 DQ[7:0] balls | 2, 3 |
| DDR0\_DQSN[0]/ DDR0\_DQSP[0] | Connect to ch0 DRAM0 DQS\_c/DQS\_t balls | 3, 4 |
| DDR0\_DQSN[1]/ DDR0\_DQSP[1] | Connect to ch0 DRAM1 DQS\_c/DQS\_t balls | 3, 4 |
| DDR0\_DQSN[2]/ DDR0\_DQSP[2] | Connect to ch0 DRAM2 DQS\_c/DQS\_t balls | 3, 4 |
| DDR0\_DQSN[3]/ DDR0\_DQSP[3] | Connect to ch0 DRAM3 DQS\_c/DQS\_t balls | 3, 4 |
| DDR0\_DQSN[4]/ DDR0\_DQSP[4] | Connect to ch0 DRAM4 DQS\_c/DQS\_t balls | 3, 4 |
| DDR0\_DQSN[5]/ DDR0\_DQSP[5] | Connect to ch0 DRAM5 DQS\_c/DQS\_t balls | 3, 4 |
| DDR0\_DQSN[6]/ DDR0\_DQSP[6] | Connect to ch0 DRAM6 DQS\_c/DQS\_t balls | 3, 4 |
| DDR0\_DQSN[7]/ DDR0\_DQSP[7] | Connect to ch0 DRAM7 DQS\_c/DQS\_t balls | 3, 4 |
| DDR1\_DQSN[0]/ DDR1\_DQSP[0] | Connect to ch0 DRAM0 DQS\_c/DQS\_t balls | 3, 4 |
| DDR1\_DQSN1]/ DDR1\_DQSP[1] | Connect to ch1 DRAM1 DQS\_c/DQS\_t balls | 3, 4 |
| DDR1\_DQSN[2]/ DDR1\_DQSP[2] | Connect to ch1 DRAM2 DQS\_c/DQS\_t balls | 3, 4 |
| DDR1\_DQSN[3]/ DDR1\_DQSP[3] | Connect to ch1 DRAM3 DQS\_c/DQS\_t balls | 3, 4 |
| DDR1\_DQSN[4]/ DDR1\_DQSP[4] | Connect to ch1 DRAM4 DQS\_c/DQS\_t balls | 3, 4 |
| DDR1\_DQSN[5]/ DDR1\_DQSP[5] | Connect to ch1 DRAM5 DQS\_c/DQS\_t balls | 3, 4 |
| DDR1\_DQSN[6]/ DDR1\_DQSP[6] | Connect to ch1 DRAM6 DQS\_c/DQS\_t balls | 3, 4 |
| DDR1\_DQSN[7]/ DDR1\_DQSP[7] | Connect to ch1 DRAM7 DQS\_c/DQS\_t balls | 3, 4 |
| DMU, DML | Tie all DRAMs DMU and DML balls directly to VDDQ. |  |
| DDR0\_VREF\_CA | Connect to VREF\_CA of Channel A (DDR0\_XXX signals)  DRAMs. Refer to System Memory Interface Design Guideline Chapter in Platform Design Guide |  |
| DDR1\_VREF\_CA | Connect to VREF\_CA of Channel B (DDR1\_XXX signals)  DRAMs. Refer to System Memory Interface Design Guideline Chapter in Platform Design Guide |  |
| DRAM\_RST# | Refer to System Memory Interface Design Guideline Chapter in Platform Design Guide |  |
| DDR\_RCOMP | Refer to System Memory Interface Design Guideline Chapter in Platform Design Guide |  |

* 1. CKP and CKN differential signal swapping within a pair is not allowed.
  2. DQ Bit Swapping is allowed within the same byte.
  3. Byte Swapping is allowed within the same channel.
  4. DQSP and DQSN differential signal swapping within a pair is not allowed.
  5. Capacitor C1 is a defensive design and should be NO STUFF by default.

### Tiger Lake UP3 and UP4 LPDDR4x Memory Down Checklist

|  |  |  |
| --- | --- | --- |
| **Pin Name** | **Schematic Notes** | **Notes** |
| DDR0\_CLK\_P | For x32 - Connect to DRAMA CK\_T\_A ball  For x64 - Connect to DRAMA CK\_Т\_0 ball | 1 |
| DDR0\_CLK\_N | For x32 - Connect to DRAMA CK\_C\_A ball  For x64 - Connect to DRAMA CK\_2\_0 ball | 1 |
| DDR1\_CLK\_P | For x32 - Connect to DRAMA CK\_T\_B ball  For x64 - Connect to DRAMA CK\_Т\_1 ball | 1 |
| DDR1\_CLK\_N | For x32 - Connect to DRAMA CK\_C\_B ball  For x64 - Connect to DRAMA CK\_2\_1 ball | 1 |
| DDR2\_CLK\_P | For x32 - Connect to DRAMB CK\_T\_A ball  For x64 - Connect to DRAMА CK\_Т\_2 ball | 1 |
| DDR2\_CLK\_N | For x32 - Connect to DRAMB CK\_C\_A ball  For x64 - Connect to DRAMА CK\_2\_2 ball | 1 |
| DDR3\_CLK\_P | For x32 - Connect to DRAMB CK\_T\_B ball  For x64 - Connect to DRAMА CK\_Т\_3 ball | 1 |
| DDR3\_CLK\_N | For x32 - Connect to DRAMB CK\_C\_B ball  For x64 - Connect to DRAMА CK\_2\_3 ball | 1 |
| DDR4\_CLK\_P | For x32 - Connect to DRAMC CK\_T\_A ball  For x64 - Connect to DRAMB CK\_Т\_0 ball | 1 |
| DDR4\_CLK\_N | For x32 - Connect to DRAMC CK\_C\_A ball  For x64 - Connect to DRAMB CK\_2\_0 ball | 1 |
| DDR5\_CLK\_P | For x32 - Connect to DRAMC CK\_T\_B ball  For x64 - Connect to DRAMB CK\_Т\_1 ball | 1 |
| DDR5\_CLK\_N | For x32 - Connect to DRAMC CK\_C\_B ball  For x64 - Connect to DRAMB CK\_2\_1 ball | 1 |
| DDR6\_CLK\_P | For x32 - Connect to DRAMD CK\_T\_A ball  For x64 - Connect to DRAMB CK\_Т\_2 ball | 1 |
| DDR6\_CLK\_N | For x32 - Connect to DRAMD CK\_C\_A ball  For x64 - Connect to DRAMB CK\_2\_2 ball | 1 |
| DDR7\_CLK\_P | For x32 - Connect to DRAMD CK\_T\_B ball  For x64 - Connect to DRAMB CK\_Т\_3 ball | 1 |
| DDR7\_CLK\_N | For x32 - Connect to DRAMD CK\_C\_B ball  For x64 - Connect to DRAMB CK\_2\_3 ball | 1 |
| DDR0\_CS[0] | For x32 - Connect to DRAMA CS0\_A ball  For x64 - Connect to DRAMA CS\_0 ball |  |
| DDR0\_CS[1] | For x32 - Connect to DRAMA CS1\_A ball  For x64 - Connect to DRAMA CS1\_0 ball |  |
| DDR1\_CS[0] | For x32 - Connect to DRAMА CS0\_B ball  For x64 - Connect to DRAMA CS\_1 ball |  |
| DDR1\_CS[1] | For x32 - Connect to DRAMА CS1\_B ball  For x64 - Connect to DRAMA CS1\_1 ball |  |
| DDR2\_CS[0] | For x32 - Connect to DRAMB CS0\_A ball  For x64 - Connect to DRAMB CS\_2 ball |  |
| DDR2\_CS[1] | For x32 - Connect to DRAMB CS1\_A ball  For x64 - Connect to DRAMB CS1\_2 ball |  |
| DDR3\_CS[0] | For x32 - Connect to DRAMB CS0\_B ball  For x64 - Connect to DRAMB CS\_3 ball |  |
| DDR3\_CS[1] | For x32 - Connect to DRAMB CS1\_B ball  For x64 - Connect to DRAMB CS1\_3 ball |  |
| DDR4\_CS[0] | For x32 - Connect to DRAMC CS0\_A ball  For x64 - Connect to DRAMB CS\_0 ball |  |
| DDR4\_CS[1] | For x32 - Connect to DRAMC CS1\_A ball  For x64 - Connect to DRAMA CS1\_0 ball |  |
| DDR5\_CS[0] | For x32 - Connect to DRAMC CS0\_B ball  For x64 - Connect to DRAMA CS\_1 ball |  |
| DDR5\_CS[1] | For x32 - Connect to DRAMC CS1\_B ball  For x64 - Connect to DRAMA CS1\_1 ball |  |
| DDR6\_CS[0] | For x32 - Connect to DRAMD CS0\_A ball  For x64 - Connect to DRAMB CS\_2 ball |  |
| DDR6\_CS[1] | For x32 - Connect to DRAMD CS1\_A ball  For x64 - Connect to DRAMB CS1\_2 ball |  |
| DDR7\_CS[0] | For x32 - Connect to DRAMD CS0\_B ball  For x64 - Connect to DRAMB CS\_3 ball |  |
| DDR7\_CS[1] | For x32 - Connect to DRAMD CS1\_B ball  For x64 - Connect to DRAMB CS1\_3 ball |  |
| DDR0\_CKE[0] | For x32 - Connect to DRAMA CKE0\_A ball  For x64 - Connect to DRAMA CKE\_0 ball |  |
| DDR0\_CKE[1] | For x32 - Connect to DRAMA CKE1\_A ball  For x64 - Connect to DRAMA CKE1\_0 ball |  |
| DDR1\_CKE[0] | For x32 - Connect to DRAMA CKE0\_B ball  For x64 - Connect to DRAMA CKE\_1 ball |  |
| DDR1\_CKE[1] | For x32 - Connect to DRAMA CKE1\_B ball  For x64 - Connect to DRAMA CKE1\_1 ball |  |
| DDR2\_CKE[0] | For x32 - Connect to DRAMB CKE0\_A ball  For x64 - Connect to DRAMA CKE\_2 ball |  |
| DDR2\_CKE[1] | For x32 - Connect to DRAMB CKE1\_A ball  For x64 - Connect to DRAMA CKE1\_2 ball |  |
| DDR3\_CKE[0] | For x32 - Connect to DRAMB CKE0\_B ball  For x64 - Connect to DRAMA CKE\_3 ball |  |
| DDR3\_CKE[1] | For x32 - Connect to DRAMB CKE1\_B ball  For x64 - Connect to DRAMA CKE1\_3 ball |  |
| DDR4\_CKE[0] | For x32 - Connect to DRAMC CKE0\_A ball  For x64 - Connect to DRAMB CKE\_0 ball |  |
| DDR4\_CKE[1] | For x32 - Connect to DRAMC CKE1\_A ball  For x64 - Connect to DRAMB CKE1\_0 ball |  |
| DDR5\_CKE[0] | For x32 - Connect to DRAMC CKE0\_B ball  For x64 - Connect to DRAMB CKE\_1 ball |  |
| DDR5\_CKE[1] | For x32 - Connect to DRAMC CKE1\_B ball  For x64 - Connect to DRAMB CKE1\_1 ball |  |
| DDR6\_CKE[0] | For x32 - Connect to DRAMD CKE0\_A ball  For x64 - Connect to DRAMB CKE\_2 ball |  |
| DDR6\_CKE[1] | For x32 - Connect to DRAMD CKE1\_A ball  For x64 - Connect to DRAMB CKE1\_2 ball |  |
| DDR7\_CKE[0] | For x32 - Connect to DRAMD CKE0\_B ball  For x64 - Connect to DRAMB CKE\_3 ball |  |
| DDR7\_CKE[1] | For x32 - Connect to DRAMD CKE1\_B ball  For x64 - Connect to DRAMB CKE1\_3 ball |  |
| DDR[3:0]\_ODT[0]/ DDR[7:4]\_ODT[1] | Not connected at CPU side |  |
| DDR0\_CA[5:0] | For x32 - Connect to DRAMA CA[5:0]\_A balls  For x64 - Connect to DRAMA CA[5:0]\_0 balls |  |
| DDR1\_CA[5:0] | For x32 - Connect to DRAMA CA[5:0]\_B balls  For x64 - Connect to DRAMA CA[5:0]\_1 balls |  |
| DDR2\_CA[5:0] | For x32 - Connect to DRAMB CA[5:0]\_A balls  For x64 - Connect to DRAMA CA[5:0]\_2 balls |  |
| DDR3\_CA[5:0] | For x32 - Connect to DRAMB CA[5:0]\_B balls  For x64 - Connect to DRAMA CA[5:0]\_3 balls |  |
| DDR4\_CA[5:0] | For x32 - Connect to DRAMC CA[5:0]\_A balls  For x64 - Connect to DRAMB CA[5:0]\_0 balls |  |
| DDR5\_CA[5:0] | For x32 - Connect to DRAMC CA[5:0]\_B balls  For x64 - Connect to DRAMB CA[5:0]\_1 balls |  |
| DDR6\_CA[5:0] | For x32 - Connect to DRAMD CA[5:0]\_A balls  For x64 - Connect to DRAMB CA[5:0]\_2 balls |  |
| DDR7\_CA[5:0] | For x32 - Connect to DRAMD CA[5:0]\_B balls  For x64 - Connect to DRAMB CA[5:0]\_3 balls |  |
| DDR0\_DQ[1:0][7:0] | For x32 - Connect to DRAMA DQ[15:0]\_A balls  For x64 - Connect to DRAMA DQ[15:0]\_0 balls | 1 |
| DDR1\_DQ[1:0][7:0] | For x32 - Connect to DRAMA DQ[15:0]\_B balls  For x64 - Connect to DRAMA DQ[15:0]\_1 balls | 1 |
| DDR2\_DQ[1:0][7:0] | For x32 - Connect to DRAMB DQ[15:0]\_A balls  For x64 - Connect to DRAMA DQ[15:0]\_2 balls | 1 |
| DDR3\_DQ[1:0][7:0] | For x32 - Connect to DRAMB DQ[15:0]\_B balls  For x64 - Connect to DRAMA DQ[15:0]\_3 balls | 1 |
| DDR4\_DQ[1:0][7:0] | For x32 - Connect to DRAMC DQ[15:0]\_A balls  For x64 - Connect to DRAMB DQ[15:0]\_0 balls | 1 |
| DDR5\_DQ[1:0][7:0] | For x32 - Connect to DRAMC DQ[15:0]\_B balls  For x64 -Connect to DRAMB DQ[15:0]\_1 balls | 1 |
| DDR6\_DQ[1:0][7:0] | For x32 - Connect to DRAMD DQ[15:0]\_A balls  For x64 - Connect to DRAMB DQ[15:0]\_2 balls | 1 |
| DDR7\_DQ[1:0][7:0] | For x32 - Connect to DRAMD DQ[15:0]\_B balls  For x64 - Connect to DRAMB DQ[15:0]\_3 balls | 1 |
| DDR0\_DQSP[0] | For x32 - Connect to DRAMA DQS0\_T\_A ball  For x64 - Connect to DRAMA DQS0\_Т\_0 ball | 2 |
| DDR0\_DQSN[0] | For x32 - Connect to DRAMA DQS0\_C\_A ball  For x64 - Connect to DRAMA DQS0\_2\_0 ball | 2 |
| DDR0\_DQSP[1] | For x32 - Connect to DRAMA DQS1\_T\_A ball  For x64 - Connect to DRAMA DQS1\_Т\_0 ball | 2 |
| DDR0\_DQSN[1] | For x32 - Connect to DRAMA DQS1\_C\_A ball  For x64 - Connect to DRAMA DQS1\_2\_0 ball | 2 |
| DDR1\_DQSP[0] | For x32 - Connect to DRAMА DQS0\_T\_B balls  For x64 - Connect to DRAMA DQS0\_Т\_1 ball | 2 |
| DDR1\_DQSN[0] | For x32 - Connect to DRAMА DQS0\_C\_B balls  For x64 - Connect to DRAMA DQS0\_2\_1 ball | 2 |
| DDR1\_DQSP[1] | For x32 - Connect to DRAMА DQS1\_T\_B balls  For x64 - Connect to DRAMA DQS1\_Т\_1 balls | 2 |
| DDR1\_DQSN[1] | For x32 - Connect to DRAMА DQS1\_C\_B balls  For x64 - Connect to DRAMA DQS1\_2\_1 balls | 2 |
| DDR2\_DQSP[0] | For x32 - Connect to DRAMB DQS0\_T\_A ball  For x64 - Connect to DRAMA DQS0\_Т\_2 ball | 2 |
| DDR2\_DQSN[0] | For x32 - Connect to DRAMB DQS0\_C\_A ball  For x64 - Connect to DRAMA DQS0\_2\_2 ball | 2 |
| DDR2\_DQSP[1] | For x32 - Connect to DRAMB DQS1\_T\_A ball  For x64 - Connect to DRAMA DQS1\_Т\_2 ball | 2 |
| DDR2\_DQSN[1] | For x32 - Connect to DRAMB DQS1\_C\_A ball  For x64 - Connect to DRAMA DQS1\_2\_2 ball | 2 |
| DDR3\_DQSP[0] | For x32 - Connect to DRAMB DQS0\_T\_B ball  For x64 - Connect to DRAMA DQS0\_Т\_3 ball | 2 |
| DDR3\_DQSN[0] | For x32 - Connect to DRAMB DQS0\_C\_B ball  For x64 - Connect to DRAMA DQS0\_2\_3 balls | 2 |
| DDR3\_DQSP[1] | For x32 - Connect to DRAMB DQS1\_T\_B ball  For x64 - Connect to DRAMA DQS1\_Т\_3 balls | 2 |
| DDR3\_DQSN[1] | For x32 - Connect to DRAMB DQS1\_C\_B ball  For x64 - Connect to DRAMA DQS1\_2\_3 balls | 2 |
| DDR4\_DQSP[0] | For x32 - Connect to DRAMB DQS0\_T\_A ball  For x64 - Connect to DRAMB DQS0\_Т\_0 ball | 2 |
| DDR4\_DQSN[0] | For x32 - Connect to DRAMB DQS0\_C\_A ball  For x64 - Connect to DRAMB DQS0\_2\_0 ball | 2 |
| DDR4\_DQSP[1] | For x32 - Connect to DRAMC DQS1\_T\_A ball  For x64 - Connect to DRAMB DQS1\_T\_0 ball | 2 |
| DDR4\_DQSN[1] | For x32 - Connect to DRAMC DQS1\_C\_A ball  For x64 - Connect to DRAMB DQS1\_2\_0 ball | 2 |
| DDR5\_DQSP[0] | For x32 - Connect to DRAMC DQS0\_T\_B ball  For x64 - Connect to DRAMB DQS0\_T\_1 ball | 2 |
| DDR5\_DQSN[0] | For x32 - Connect to DRAMC DQS0\_C\_B ball  For x64 - Connect to DRAMB DQS0\_2\_1 ball | 2 |
| DDR5\_DQSP[1] | For x32 - Connect to DRAMC DQS1\_T\_B ball  For x64 - Connect to DRAMB DQS1\_T\_1 ball | 2 |
| DDR5\_DQSN[1] | For x32 - Connect to DRAMC DQS1\_C\_B ball  For x64 - Connect to DRAMB DQS1\_2\_1 ball | 2 |
| DDR6\_DQSP[0] | For x32 - Connect to DRAMD DQS0\_T\_A ball  For x64 - Connect to DRAMB DQS0\_T\_2 ball | 2 |
| DDR6\_DQSN[0] | For x32 - Connect to DRAMD DQS0\_C\_A ball  For x64 - Connect to DRAMB DQS0\_2\_2 ball | 2 |
| DDR6\_DQSP[1] | For x32 - Connect to DRAMD DQS1\_T\_A ball  For x64 - Connect to DRAMB DQS1\_T\_2 ball | 2 |
| DDR6\_DQSN[1] | For x32 - Connect to DRAMD DQS1\_C\_A ball  For x64 - Connect to DRAMB DQS1\_2\_2 ball | 2 |
| DDR7\_DQSP[0] | For x32 - Connect to DRAMD DQS0\_T\_B ball  For x64 - Connect to DRAMB DQS0\_T\_3 ball | 2 |
| DDR7\_DQSN[0] | For x32 - Connect to DRAMD DQS0\_C\_B ball  For x64 - Connect to DRAMB DQS0\_2\_3 ball | 2 |
| DDR7\_DQSP[1] | For x32 - Connect to DRAMD DQS1\_T\_B ball  For x64 - Connect to DRAMB DQS1\_T\_3 ball | 2 |
| DDR7\_DQSN[1] | For x32 - Connect to DRAMD DQS1\_C\_B ball  For x64 - Connect to DRAMB DQS1\_2\_3 ball | 2 |
| DDR0\_PAR/ DDR1\_PAR# | Not used at LPDDR4x. Not connected at processor side. |  |
| DDR0\_ALERT#/ DDR1\_ALERT# | Not used at LPDDR4x. Tied to GND or not connected. |  |
| DMI[1:0] | For x32 -Tie DRAMA,DRAMB,DRAMC and DRAMD DMI[1:0]\_A  and DMI[1:0]\_B balls directly to ground  For x64- Tie DRAMA and DRAMB DMI[1:0]\_A, DMI[1:0]\_B, |  |
| DDR0\_VREF\_CA/ DDR1\_VREF\_CA | Not connected |  |
| DRAM\_RST# | Refer to System Memory Interface Design Guideline Chapter in Platform Design Guide |  |
| DDR\_RCOMP | Refer to System Memory Interface Design Guideline Chapter in Platform Design Guide |  |

* 1. CKP and CKN differential signal swapping within a pair is not allowed. Also, differential clock pair to clock pair swapping within a channel is not allowed.
  2. DQSP and DQSN differential signal swapping within a pair is not allowed.

## USB Type C

Table 1. Type C High Speed Differentials Checklist

|  |  |  |  |
| --- | --- | --- | --- |
| **Function** | **Port** | **Pin Name** | **Schematic Notes** |
| High Speed Differential | Port 0 | TCP0\_TX\_P0 | Integrated TBT: Refer Burnside Bridge retimer reference design for retimer circuit and PDG for topology guidelines.  Type C Direct(USB+DP): Refer PDG for topology guidelines. |
| TCP0\_TX\_N0 |
| TCP0\_TX\_P1 |
| TCP0\_TX\_N1 |
| TCP0\_TXRX\_P0 |
| TCP0\_TXRX\_N0 |
| TCP0\_TXRX\_P1 |
| TCP0\_TXRX\_N1 |
| Port 1 | TCP1\_TX\_P0 |
| TCP1\_TX\_N0 |
| TCP1\_TX\_P1 |
| TCP1\_TX\_N1 |
| TCP1\_TXRX\_P0 |
| TCP1\_TXRX\_N0 |
| TCP1\_TXRX\_P1 |
| TCP1\_TXRX\_N1 |
| Port 2 | TCP2\_TX\_P0 |
| TCP2\_TX\_N0 |
| TCP2\_TX\_P1 |
| TCP2\_TX\_N1 |
| TCP2\_TXRX\_P0 |
| TCP2\_TXRX\_N0 |
| TCP2\_TXRX\_P1 |
| TCP2\_TXRX\_N1 |
| Port 3 | TCP3\_TX\_P0 |
| TCP3\_TX\_N0 |
| TCP3\_TX\_P1 |
| TCP3\_TX\_N1 |
| TCP3\_TXRX\_P0 |
| TCP3\_TXRX\_N0 |
| TCP3\_TXRX\_P1 |
| TCP3\_TXRX\_N1 |
| NOTE: PORT 3 available on TGL-UP3 only. | | | |

Table 2. Type C Auxiliary and Sideband Checklist

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Function** | **Port** | **Alternate Mode Pin Name** | **Thunderbolt™ Mode Pin Name** | **Schematic Notes** |
| Auxiliary and Thunderbolt™ Sideband | Port 0 | TCP0\_AUXPAD\_N | GPP\_E18 / TBT\_LSX0\_TXD | Refer TGL U DDR4 CRB schematics for Type C Direct Auxiliary signal connect orientations.  AC caps are needed for Type C direct implementations on Auxiliary signals.  Refer CRB schematics for LSx signal connections. |
| TCP0\_AUXPAD\_P | GPP\_E19 / TBT\_LSX0\_RXD |
| Port 1 | TCP1\_AUXPAD\_N | GPP\_E20 / TBT\_LSX1\_TXD |
| TCP1\_AUXPAD\_P | GPP\_E21 / TBT\_LSX1\_RXD |
| Port 2 | TCP2\_AUXPAD\_N | GPP\_D9 / TBT\_LSX2\_TXD |
| TCP2\_AUXPAD\_P | GPP\_D10 / TBT\_LSX2\_RXD |
| Port 3 | TCP3\_AUXPAD\_N | GPP\_D11/ TBT\_LSX3\_TXD |
| TCP3\_AUXPAD\_P | GPP\_D12 / TBT\_LSX3\_RXD |
| NOTE: PORT 3 available on TGL-UP3 only. | | | | |

Table 3 TCP Disabling and Termination Guidelines

|  |  |
| --- | --- |
| **Pin name** | **Recommendation** |
| **TCPx\_TX\_N/P[1:0]**  **TCPx\_TXRX\_N/P [1:0]** | No connect |
| **TCPx\_AUX\_N/P** | No connect |
| **TC\_RCOMP\_N**  **TC\_RCOMP\_P** | 150Ω+/-1% between TC\_RCOMP\_N and TC\_RCOMP\_P. Provide good noise isolation. Platform Rdc < 0.5 Ohm for the sum of both signals. |

Table 4. Type C Low Speed and RCOMP Checklist

|  |  |  |  |
| --- | --- | --- | --- |
| **Function** | **Port** | **Pin Name** | **Schematic Notes** |
| Low Speed Differential | Port 0 | USB2N\_[1:10] | Can be any of the USB2 ports from the PCH [1- 10] |
| USB2P\_[1:10] |
| Port 1 | USB2N\_[1:10] |
| USB2P\_[1:10] |
| Port 2 | USB2N\_[1:10] |
| USB2P\_[1:10] |
| Port 3 | USB2N\_[1:10] |
| USB2P\_[1:10] |
| Resistor Compensation | All | TC\_RCOMP\_N | 150Ω+/-1% between TC\_RCOMP\_N and TC\_RCOMP\_P. Provide good noise isolation. Platform Rdc < 0.5 Ohm for the sum of both signals. |
| TC\_RCOMP\_P |
| **NOTE:** Port 3 available on TGL-UP3 only. | | | |

Table 5. Type C Power, Ground, and Control Checklist

|  |  |  |  |
| --- | --- | --- | --- |
| **Function** | **Port** | **Pin Name** | **Schematic Notes** |
| Power | All | VBUS | VBUS, capable of up to 5A @ 20V with USB PD |
| VCONN | VCONN is a power source to active cable which can supply up to 0.2A @ 5V. Unconnected CC pin will be reconfigured to VCONN when a device is plugged in. |
| Ground | All | GND | Ground |
| Configuration Channels | All | CC1 | Configuration Channel 1. Used for device detection, orientation detection and Alternate Mode configuration. Unconnected pins will be reconfigured to Vconn. |
| CC2 | Configuration Channel 2. Used for device detection, orientation detection and Alternate Mode configuration. Unconnected pins will be reconfigured to Vconn. |
| **NOTE:** Port 3 available on TGL-UP3 only. | | | |

## Digital Display

Table 6. DisplayPort (DP) Checklist

|  |  |  |  |
| --- | --- | --- | --- |
| **Port** | **Function** | **DDI Signal Name** | **DP Signal Name** |
| DDI B | Main Link | DDIB\_TXP[0] | DDIB\_DP\_LANE0\_P |
| DDIB\_TXN[0] | DDIB\_DP\_LANE0\_N |
| DDIB\_TXP[1] | DDIB\_DP\_LANE1\_P |
| DDIB\_TXN[1] | DDIB\_DP\_LANE1\_N |
| DDIB\_TXP[2] | DDIB\_DP\_LANE2\_P |
| DDIB\_TXN[2] | DDIB\_DP\_LANE2\_N |
| DDIB\_TXP[3] | DDIB\_DP\_LANE3\_P |
| DDIB\_TXN[3] | DDIB\_DP\_LANE3\_N |
| Aux | DDIB\_AUX\_P | DDIB\_DP\_AUX\_P |
| DDIB\_AUX\_N | DDIB\_DP\_AUX\_N |
| HPD | DDSP\_HPDB | DPB\_HPD |
| Type C x | Main Link | TCPx\_TX\_N0 | DDIx\_DP\_LANE0\_N |
| TCPx\_TX\_P0 | DDIx\_DP\_LANE0\_P |
| TCPx\_TX\_N1 | DDIx\_DP\_LANE2\_N |
| TCPx\_TX\_P1 | DDIx\_DP\_LANE2\_P |
| TCPx\_TXRX\_N0 | DDIx\_DP\_LANE1\_N |
| TCPx\_TXRX\_P0 | DDIx\_DP\_LANE1\_P |
| TCPx\_TXRX\_N1 | DDIx\_DP\_LANE3\_N |
| TCPx\_TXRX\_P1 | DDIx\_DP\_LANE3\_P |
| Aux | TCPx\_AUX\_P | DDIx\_DP\_AUX\_P |
| TCPx\_AUX\_N | DDIx\_DP\_AUX\_N |
| HPD | DDSP\_HPDx | DPx\_HPD |
| ALL | RCOMP | DISP\_RCOMP | Pull Down to VSS via 150 Ohm resistor |
| ALL | UTILS | DISP\_UTILS | Recommend 50 Ω nominal trace impedance with reasonable noise isolation. Requires level shifting on the platform. |
| ALL2 | Dual Mode | AUX Enable | DDIx/B\_AUX\_EN |
| * 1. x can be port 1-4 depend on the SKU.   2. Optional for AUX channel dual mode protection support. Refer PDG for DisplayPort Auxiliary Channel Dual Mode Support Protection Circuit | | | |

Table 7. HDMI Checklist

|  |  |  |  |
| --- | --- | --- | --- |
| **Port** | **Function** | **DDI Signal Name** | **HDMI\* Signal Name** |
| DDI B | Main Link | DDIB\_TXP[0] | DDIB\_HDMI\_DATA2\_P |
| DDIB\_TXN[0] | DDIB\_HDMI\_DATA2\_N |
| DDIB\_TXP[1] | DDIB\_HDMI\_DATA1\_P |
| DDIB\_TXN[1] | DDIB\_HDMI\_DATA1\_N |
| DDIB\_TXP[2] | DDIB\_HDMI\_DATA0\_P |
| DDIB\_TXN[2] | DDIB\_HDMI\_DATA0\_N |
| DDIB\_TXP[3] | DDIB\_HDMI\_CLK\_P |
| DDIB\_TXN[3] | DDIB\_HDMI\_CLK\_N |
| DDC | DDPB\_CTRLCLK | DDIx\_HDMI\_OB\_SCL |
| DDPB\_CTRLDATA | DDIx\_HDMI\_OB\_SDA |
| HPD | DDSP\_HPDB | HDMIB\_HPD |
| Type C x | Main Link | TCPx\_TX\_N0 | DDIx\_HDMI\_DATA2\_N |
| TCPx\_TX\_P0 | DDIx\_HDMI\_DATA2\_P |
| TCPx\_TX\_N1 | DDIx\_HDMI\_DATA0\_N |
| TCPx\_TX\_P1 | DDIx\_HDMI\_DATA0\_P |
| TCPx\_TXRX\_N0 | DDIx\_HDMI\_DATA1\_N |
| TCPx\_TXRX\_P0 | DDIx\_HDMI\_DATA1\_P |
| TCPx\_TXRX\_N1 | DDIx\_HDMI\_CLK\_N |
| TCPx\_TXRX\_P1 | DDIx\_HDMI\_CLK\_P |
| DDC | DDPx\_CTRLCLK | DDIx\_HDMI\_OB\_SCL |
| DDPx\_CTRLDATA | DDIx\_HDMI\_OB\_SDA |
| HPD | DDSP\_HPDx | HDMIx\_HPD |
| ALL | RCOMP | DISP\_RCOMP | Pull Down to VSS via 150 Ohm resistor |
| **NOTE:** x can be port 1-4 depend on the SKU. | | | |

Table 8. eDP Checklist

|  |  |  |  |
| --- | --- | --- | --- |
| **Port** | **Function** | **DDI Signal Name** | **eDP\* Signal Name** |
| DDIA/B | Main Link | DDIx\_TXP[0] | DDIx\_eDP\_LANE0\_P |
| DDIx\_TXN[0] | DDIx\_eDP\_LANE0\_N |
| DDIx\_TXP[1] | DDIx\_eDP\_LANE1\_P |
| DDIx\_TXN[1] | DDIx\_eDP\_LANE1\_N |
| DDIx\_TXP[2] | DDIx\_eDP\_LANE2\_P |
| DDIx\_TXN[2] | DDIx\_eDP\_LANE2\_N |
| DDIx\_TXP[3] | DDIx\_eDP\_LANE3\_P |
| DDIx\_TXN[3] | DDIx\_eDP\_LANE3\_N |
| Aux | DDIx\_AUX\_P | DDIx\_eDP\_AUX\_P |
| DDIx\_AUX\_N | DDIx\_eDP\_AUX\_N |
| RCOMP | DISP\_RCOMP | Pull Down to VSS via 150 ohm resistor |
| UTILS | DISP\_UTILS | Recommend 50 Ω nominal trace impedance with reasonable noise isolation.  Requires level shifting on the platform. |
| HPD | DDSP\_HPDA - DDIA DDSP\_HPDB - DDIB | eDPA\_HPD eDPB\_HPD |
| VDD Enable | EDP\_VDDEN - DDIA GPP\_A17 - DDIB | eDPA\_VDDEN eDPB\_VDDEN |
| BKLT Enable | EDP\_BKLTEN - DDIA GPP\_A21 - DDIB | eDPA\_BKLT\_EN eDPB\_BKLT\_EN |
| BKLT Control | EDP\_BKLTCTL - DDIA GPP\_A22 - DDIB | eDPA\_BRIGHTNESS eDPB\_BRIGHTNESS |
| **NOTE:** x can be DDI port A or B. | | | |

Table 9 Disabling and Termination Guidelines

|  |  |
| --- | --- |
| **Pin name** | **Recommendation** |
| **DDIx\_TXN/P[3:0]** | No connect |
| **DDIx\_AUXN/P** | No connect |
| **DDIx\_HPD** | Pull down to ground via 100k Ω resistor |
| **DDIA\_RCOMP** | Pull Down to VSS via 150 Ohm resistor. |
| **DISP\_UTIL / DSI\_DE\_TE\_1** | No connect |
| **DSI\_DE\_TE\_2** | 100K Ohm to ground. |

## Processor PCI Express\* Checklist

|  |  |  |
| --- | --- | --- |
| **Pin Name** | **Schematics Notes** |  |
| PCIE4\_RX\_P[3:0]  PCIE4\_RX\_N[3:0] PCIE4\_TX\_P[3:0]  PCIE4\_TX\_N[3:0] | PCI Express\* Device Down Details  Connect PCIE4\_Tx PCIe\* balls through an AC Coupling Capacitor in the following range:  Gen3/4 = 75 to 265 nF; where 220 nF is nominal value |  |
| PCIE4\_RCOMPN PCIE4\_RCOMPP | External resistor between RCOMPP/RCOMPN |  |
| **NOTE:** Any PCI Express\* Transmit and associated Receive Differential Pair not being used or implemented on the platform must be left as no connects. | | |

## CPU Sideband Signals

|  |  |  |  |
| --- | --- | --- | --- |
| **Pin Name** | **System Pull-up/ Pull-down** | **Schematics Notes** |  |
| PECI | 43 Ω series resistor to EC |  |  |
| THRMTRIP# | 1 KΩ Pull-up to VCCST | For TGL Y connect to VCCST\_OUT |  |
| VCCSTPWRGOOD\_TCSS | 50-100 KΩ Pull-downs | Processor pin Before VCCST FET |  |
| VCCST\_OVERRIDE | 50-100 KΩ Pull-downs | PCH Pin connect with Processor pin VCCSTPWRGOOD\_TCSS before VCCST FET |  |
| VCCST\_PWRGD | 62Ω series resistor to 1 KΩ Pull- up to VCCST | Refer VCCST\_PWRGOOD Chapter in PDG  For TGL Y connect to VCCST\_OUT |  |
| CATERR# | 1 kΩ Pull-up to VCCST | For TGL Y connect to VCCST\_OUT |  |
| PROCHOT# | 500Ω series resistor to 1 KΩ Pull-up to VCCSTG | Another few resistors depends on number of agents refer PROCHOT# Chapter in PDG  For TGL Y connect to VCCSTG\_OUT |  |
| VIDSOUT | Rpu1=100Ω, Rpu2=100Ω | Refer SVID Chapter in PDG  For TGL Y connect to VCCST\_OUT |  |
| VIDSCK | Rpu1=N/A, Rpu2=45 Ω |  |
| VIDSALERT# | Rpu1=56 Ω, Rpu2=N/A |  |

## CSI and Imaging Clock

|  |  |
| --- | --- |
| **Pin Name** | **Schematic Notes** |
| CSI\_C\_DN[0] | Connect directly to device/connector |
| CSI\_C\_DP[0] |
| CSI\_D\_DN[3:0] |
| CSI\_D\_DP[3:0] |
| CSI\_E\_DN[1:0] |
| CSI\_E\_DP[1:0] |
| CSI\_F\_DN[1:0] |
| CSI\_F\_DP[1:0] |
| CSI\_G\_DN[0] |
| CSI\_G\_DP[0] |
| CSI\_H\_DN[3:0] |
| CSI\_H\_DP[3:0] |
| CSI\_C\_CLK\_N | Connect directly to device/connector |
| CSI\_C\_CLK\_P |
| CSI\_D\_CLK\_N |
| CSI\_D\_CLK\_P |
| CSI\_E\_CLK\_N |
| CSI\_E\_CLK\_P |
| CSI\_F\_CLK\_N |
| CSI\_F\_CLK\_P |
| CSI\_G\_CLK\_N |
| CSI\_G\_CLK\_P |
| CSI\_H\_CLK\_N |
| CSI\_H\_CLK\_P |
| CSI\_A\_DN[1:0] | Connect directly to device/connector (TGL-Y Only) |
| CSI\_A\_DP[1:0] |
| CSI\_A\_CLK\_N |
| CSI\_A\_CLK\_P |
| CSI\_RCOMP | External Reference resistor compensation (150 Ω ±1% To GND) |
| GPP\_D4 / IMGCLKOUT0 | Camera Clock, Connect directly to device/connector |
| GPP\_H20 / IMGCLKOUT1 |
| GPP\_H21 / IMGCLKOUT2 |
| GPP\_H22 / IMGCLKOUT3 |
| GPP\_H23 / IMGCLKOUT4 |
| GPP\_D15 / ISH\_UART0\_RTS# / GSPI2\_CS1# / IMGCLKOUT5 |
| **Note:** Polarity (P/N) cannot be reversed | |

## Platform Clock

Table 10. Platform Clock Checklist

|  |  |  |
| --- | --- | --- |
| **Pin Name** | **Schematics Notes** |  |
| TGL UP3 PCH-LP: CLKOUT\_PCIE\_P[6:0] CLKOUT\_PCIE\_N[6:0]  TGL UP4 PCH-LP: CLKOUT\_PCIE\_P[4:0] CLKOUT\_PCIE\_N[4:0] | Direct connect 100 MHz differential PCIe\* output clocks to PCIe\* connector pins or device down balls.  **NOTES:**   * 1. Any differential clock pair not being used must be left as no connect and its associated clock buffer must be disabled by means of the Intel® Management Engine (Intel® ME) FW. Refer to Intel® ME FW Bring Up Guide for configuring/disabling details.   2. CLKOUT\_PCIE\_P /N [6:4, 2:1] = Support up to PCIe\* Gen3   3. CLKOUT\_PCIE\_P /N [3, 0] = Support up to PCIe\* Gen4 |  |
| Modem\_CLKREQ | CNVi-CRF Init flow indication: Connect to JFP device balls with a 10 KΩ  ±10% Pull Down resistor |  |
| TGL UP3 PCH-LP:  SRCCLKREQ#[6:0]  TGL UP4 PCH-LP: | Any used, enabled, and mapped SRCCLKREQ# signal should connect to a PCIe\* connector pin or a device down ball with a 10K Ohm ±10% external pull-up resistor to core rail. |  |
| SRCCLKREQ#[5:0] | Any un-used, disabled, and non-mapped SRCCLKREQ# signal must be left as no connects at the PCH side on the platform.  Notes:  The SRCCLKREQ# signals can be configured to map to any of the PCH PCI Express\* Root Ports while using any of the CLKOUT\_PCIE\_P/N differential pairs |
| XTAL\_IN XTAL\_OUT | Connect to external 38.4-MHz Crystal oscillator circuit along with 15pF external load capacitors and 200k Ohm ± 1% Bias resistor, R1 -0 Ohm, R2 – 0 Ohm. For complete details, refer “Platform Clocks Design Guideline” chapter in PDG. |  |
| XCLK\_BIASREF | Connect to an external precision 60 Ohm ±1.0% resistor to GND |  |

## RTC Circuit

Table 11. RTC Checklist

|  |  |  |
| --- | --- | --- |
| **Pin Name** | **Schematics Notes** | **** |
| RTCX1, RTCX2 | Connect a 32.768 KHz crystal oscillator across these pins with a 10 M resistor and decoupling capacitors. Values for C1 and C2 are dependent on crystal vendor recommendations. Typical values of C1 and C2 are 18 pF, based on a crystal load of 12.5 pF. |  |
| RTCRST# | An RC delay circuit with a time delay in the range of 18–25 ms should be provided. The recommended values for resistor and capacitor are 20 KΩ and 1.0 µF. The circuit should be connected to VCCRTC. |  |
| SRTCRST# | An RC delay circuit with a time delay in the range of 18–25 ms should be provided. CRB uses 20 KΩ and 1.0 µF for resistor and capacitor. The circuit should be connected to VCCRTC |  |
| INTRUDER# | A 1 MΩ pull-up is used on the customer reference board (CRB). This is needed to reduce leakage from Coin Cell Battery in G3 state. |  |
| **NOTE:** For further information on RTC, refer to the Real Time Clock Chapter in PDG. | | |

## PCH PCI Express\*

Table 12. PCI Express\* Checklist

|  |  |  |
| --- | --- | --- |
| **Pin Name** | **Schematics Notes** |  |
| UP3:  PCIE[12:1]\_TXN PCIE[12:1]\_TXP  UP4:  PCIE[12:7, 4:1]\_TXN  PCIE[12:7, 4:1]\_TXP | PCI Express\* Device Down Details:  Connect to PERpx/PERnx PCIe\* device balls through a 0402 or 0603 AC Coupling Capacitor in the following ranges:   * Gen1 and Gen2 = 75 to 200 nF; where 100 nF is nominal value * Gen3 = 176 to 265 nF; where 220 nF is nominal value   **NOTE:** No chip pack capacitors allowed  PCI Express Connector/Internal Cable Details:  Connect to HSOPx/HSONx PCIe\* connector pins through a 0402 or 0603 AC Coupling Capacitor in the following ranges:   * Gen1 and Gen2 = 75 to 200 nF; where 100 nF is nominal value * Gen3 (Connector Only) = 176 to 265 nF; where 220 nF is nominal value   **NOTE:** No chip pack capacitors allowed |  |
| UP3:  PCIE[12:1]\_RXN PCIE[12:1]\_RXP  UP4:  PCIE[12:7, 4:1]\_RXN  PCIE[12:7, 4:1]\_RXP | PCI Express\* Device Down Details:  Connect to PETpx/PETnx PCIe\* device balls through a 0402 or 0603 AC Coupling Capacitor in the following ranges:   * Gen1 and Gen2 = 75 to 200 nF; where 100 nF is nominal value * Gen3 = 176 to 265 nF; where 220 nF is nominal value   **NOTE:** No chip pack capacitors allowed  PCI Express Connector/Internal Cable Details:  Connect to HSIPx/HSINx PCIe\* connector pins. No motherboard AC Coupling Capacitors are needed since they reside on the add-in cards. |  |
| PCIE\_RCOMPN PCIE\_RCOMPP | 100 Ohm +/-1.0% external resistor between RCOMPP/RCOMPN |  |
| **NOTE:** Any PCI Express\* Transmit and associated Receive Differential Pair not being used or implemented on the platform must be left as no connects. | | |

## HSIO Serial ATA

|  |  |  |
| --- | --- | --- |
| **Pin Name** | **System Pull-up/ Pull-down** | **Notes** |
| SATAx\_TXP/TXN, SATAx\_RXP/RXN | NA | Use 10 nF with ±15% tolerance series AC-coupling- capacitors between PCH and SATA connector. Connect AC Coupling capacitors as close as possible to SATA connector, maximum distance from connector is 500 mils.  Must be of single component type X7R capacitor with body size 0402. |
| SATA\_LED# | Needs a weak pull-up. 10 KΩ ±10% pull-Up to V3.3. | The SATA\_LED# signal is open-collector and requires a weak external pull-up (8.2–10 KΩ) to +Vcc3\_3.  This is an open-collector output pin driven during SATA command activity. It is to be connected to external circuitry that can provide the current to drive a platform LED. When active, the LED is on. When tri-stated, the LED is off. An external pull-up resistor is required.  Circuit design to drive LED must limit excessive current drain to PCH SATA\_LED# pin. |
| DEVSLP |  | DEVSLP is a level triggered signal, asserted high to enable DEVSLP.  **NOTES:**   * + DEVSLP is 3.3V tolerant.   + This is an open-drain pin on the PCH side. PCH will tri- state this pin to signal to the SATA device that it may enter a lower power state (pin will go high due to   + pull-up that’s internal to the SATA device, per DEVSLP specification). PCH will drive pin low to signal an exit from DEVSLP state.   + When used as DEVSLP, no external pull-up or pull- down termination required from SATA Host DEVSLP.   + The device shall tolerate the DEVSLP signal being shorted to ground. The device shall tolerate a no connect floating DEVSLP signal. |
| RCOMP |  | SATA compensation circuit is code share with PCIE\_RCOMPP/N differential pair. Refer to PCI Express Design Guidelines chapter for PCIE\_RCOMPP/N guideline. |
| SATAGP | 10 KΩ ±10% pull-up to V3.3 | The Device Present pin on a SATA slim-line device is routed to the respective SATAGP pin in PCH or EC which is connected to the AHCI mechanical presence switch of the SATA port to support SATA slim-line connectors, SATA repeaters, and docking connectors in order to detect hot plug events. The PCH is required to pull-up the Device Present pin to 3.3 volts by means of a 10 KΩ pull-up resistor.  If MPS/interlock switches are not required, this pin can be configured as GPIO.  Unused SATAGP pins can be left as no connect and need to be default to GPIO functionality, refer to an unused GPIO for termination guidance. |
| GPIO | 10 KΩ ±10%  pull-up to V3.3 | The MD/DA on a slim-line ODD shall be connected to a level- triggered PCH GPIO Input Pin. This GPIO must be capable of generating an SCI event. The PCH is required to pull-up the MD/ DA pin to 3.3 volts by means of a 10 KΩ pull-up resistor. |
| GPIO |  | A PCH GPIO is required to control the FET switch which powers on/ off the ODD device. |

## USB 3.2 Guidelines

The PCH chipset has support for up to 4 SuperSpeed USB 3.2 capable ports by means of the XHCI controller. A single USB 3.2 connector will have 3.2 signals, USB 2.0 signals, and an overcurrent signal routed to it as shown in table below.

Table 13. PCH USB Port Mapping

|  |  |  |
| --- | --- | --- |
| **Overcurrent Pins** | **Mapping** | **SKU** |
| OC0# | Refer to Tiger Lake Processor Family External Design Specifications EDS for OC mapping. | U, Y |
| OC1# | U, Y |
| OC2# | U, Y |
| OC3# | U, Y |

Table 14. USB 3.2 Guidelines Checklist

|  |  |  |  |
| --- | --- | --- | --- |
| **Pin Name** | **System Pull-up/ Pull-down** | **Schematics Notes** |  |
| USB31\_x\_TXP, USB31\_x\_TXN, USB31\_x\_RXP, USB31\_x\_RXN |  | USB 3.2 transmit pairs require a 75–265 nF capacitor in the path between PCH and ESD/CMC protection.  The capacitor value is an Absolute range, including part tolerances.  Ensure appropriate ESD and EMI suppression devices are in place. Refer to the Universal Serial Bus USB 3.2 Gen1 and Gen2 Design Guidelines section in Tiger Lake Platform - Design Guide.  Make sure that CMC footprint is identical to a zero Ω resistor. Unused USB ports can be left as no connect. |  |

### USB Disabling and Termination Guidelines

If a USB port(s) is not implemented on the platform:

* USBP [x]P/N signals can be left unconnected
* OC [x]# pins require a pull-up to V3.3A with 8.2–10 KΩ resistors

### Overcurrent Pin Default Usage

The following table shows the default configuration for the OC (overcurrent) pins. Each OC pin is configured to protect one or more USB ports.

Table 15. Overcurrent Pin Default Usage Checklist

|  |  |  |
| --- | --- | --- |
| **Overcurrent Pin** | **PCH Mapping** | **SKU** |
| OC0# | Refer to Tiger Lake Processor Family External Design Specifications EDS for OC port mapping. | -LP |
| OC1# | -LP |
| OC2# | -LP |
| OC3# | -LP |

## USB 2.0

Table 16. USB Interface Checklist

|  |  |  |  |
| --- | --- | --- | --- |
| **Pin Name** | **System Pull-up/ Pull-down** | **Schematics Notes** |  |
| USB2P, USB2N |  | Ensure appropriate ESD and EMI suppression devices are in place.  Unused USB ports can be left as no connect due to internal pull-down resistors. |  |
| OC[x]# | 10 KΩ pull-up to V3.3A power-rail | When configured as OC[x], 10 KΩ pull-up to V3.3A power-rail is required.  When this pin is configured as GPIO, no pull up is required.  **NOTES:**   * + OC# pins are not 5V tolerant.   + OC# pins must be shared between ports.   + Each USB Connector should be protected by only one OC line. |  |
| USB2\_COMP | 113 Ω ±1% pull-down to GND. | Connect signals together and pull-down through a common resistor.  No other resistor value can be used. |  |

## Audio

Table 17. Intel® High Definition Audio (Intel® HD Audio) Interface Checklist

| Pin Name | System Pull-up/ Pull- down | Series Termination Resistor | Schematics Notes |  |
| --- | --- | --- | --- | --- |
| HDA\_RST# | None | 33 Ω | Connected between PCH and Intel® High Definition Audio (Intel® HD Audio) codec. A series-termination- resistor is required for connection to a codec. |  |
| HDA\_SYNC | Internal pull- down | 33 Ω | Connected between PCH and Intel® HD Audio codec. A series-termination-resistor is required for connection to a codec.  There is a weak integrated pull-down resistor on the HDA\_SYNC pins |  |
| HDA\_BCLK | None | 33 Ω | Connected between PCH and Intel® HD Audio codec. HDA\_BIT\_CLK (24 MHz) is output from the PCH to a codec present on the link. |  |
| HDA\_SDO | None | 33 Ω | Connected between PCH and Intel® HD Audio codec. A series-termination-resistor is required for connection to a codec.  This is also used as strap where the Flash Descriptor Security Override/Intel® ME Debug Mode if strap is sampled low, the security measures defined in the Flash Descriptor will be in effect (default). If sampled high, the Flash Descriptor Security will be overridden.  This strap should only be asserted high by means of an external pull-up to 3.3A rail in manufacturing/ debug environments ONLY.   1. Asserting the HDA\_SDO high on the rising edge of PWROK will also halt Intel® ME after chipset bring up and disable runtime Intel® ME features. This is a debug mode and must not be asserted after manufacturing/debug. |  |
| HDA\_SDIN [1:0] | Internal Pull- Down | 33 Ω | Connected between PCH and HD Audio codec. Can be left NO CONNECT, if not used (internal pull-down resistors that are always enabled). |  |
| VCCHDA  Refer Note#2 | None | None. Refer  Note 2. | This rail needs to be connected to the 3.3V power-rail or 1.8V power-rail.  Also, a 0.1-μF capacitor is required, close to the PCH ball |  |
| * 1. 33-series-termination-resistors are required on HDA\_SDIN [1:0]. If the series-resistors are not already on the Intel® HD Audio codec connector the series-resistors should be placed on the motherboard, as close as possible to the connector or 3rd party device.   2. VCCHDA is used for HD Audio and I2S interfaces for 3.3V or 1.8 V link voltages. Please ensure VCCHDA matches the end devices IO voltage settings. | | | | |

Table 18. Intel® DMIC Interface Checklist

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Pin Name | System Pull-up/ Pull-down | Series Termination Resistor | Schematics Notes |  |
| DMIC\_CLK[1:0] | None | 33 Ω | Connect each clock signal to up to two DMIC devices (stereo mics for each DATA signal) with series resistor connected close to PCH. An additional 27pF cap placeholder recommended to be placed as close to series resistor in case EMI/RFI protection is needed. |  |
| DMIC\_DATA[1:0] | Internal pull-down | 33 Ω | Connect each data signal to up to two DMIC devices (stereo mics for each DATA signal) with series resistor connected close to DMIC device |  |

Table 19. Intel® I2S Interface Checklist

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Pin Name** | **System Pull-up/ Pull-down** | **Series Termination Resistor** | **Schematics Notes** |  |
| I2S\_MCLK | None | 33 Ω | Connected between PCH and I2S devices. Series resistor should be connected close to the PCH. |  |
| I2S[5:0]\_SCLK | Internal pull-down | 33 Ω |  |
| I2S[5:0]\_TXD | Internal pull-down | 33 Ω |  |
| I2S[5:0]\_RXD | Internal pull-down | 33 Ω |  |
| I2S[5:0]\_SFRM | Internal pull-down | 33 Ω |  |

Table 20. SoundWire\* Checklist

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Pin Name** | **System Pull-up/ Pull-down** | **Series Termination Resistor** | **Schematics Notes** | **** |
| SNDW[4:1]\_CLK | None | 1 load with cables - Single 0 Ω resistor between PCH and device connector  2 load star topology with cables – Two 0 Ω resistors with one between PCH and each load connector  2 load daisy chain topology with cables – Single 13 Ω resistor between PCH and device connectors   4 load daisy chain topology with cables – Single 10 Ω resistor between PCH and device connectors  1 load topology with device down on main board – Single 0 Ω resistor between PCH and device  3 load daisy chain topology with devices down on main board – Single 0 Ω resistor between PCH and devices  4 load daisy chain topology with devices down on main board - Single 0 Ω resistor between PCH and devices | Connected between PCH and SoundWire devices. Series resistor should be connected close to the PCH. |  |
| SNDW[4:1]\_DATA | Internal pull- down |  |

## Serial Peripheral Interface (SPI)

Table 21. Strap Requirement Checklist

|  |  |  |  |
| --- | --- | --- | --- |
| Signal | Strap Pull-Up | Schematics Notes | **** |
| SPI0\_MOSI | 4.7K PU | External pull-up is required. Recommend 4.7 kohm pull up.  This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling. |  |
| SPI0\_IO2 | 100K PU to 3.3 V or  75K PU to 1.8 V | External pull-up is required. Recommend 100K if pulled up to 3.3 V or 75K if pulled up to 1.8 V.  This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling. |  |
| SPI0\_IO3 | 100K PU to 3.3 V or  75K PU to 1.8 V |  |

Table 22. SPI Topology Checklist

| Pin Name | System Pull-up/ Pull- down | Series Termination Resistor | Notes |
| --- | --- | --- | --- |
| SPI0\_MISO, SPI0\_MOSI, SPI0\_CLK, SPI0\_IO2, SPI0\_IO3 |  | 50 Ω/ 33 Ω/ 75 Ω/ 15 Ω/ 10 Ω/ 5 Ω/ 0 Ω | SPI input/output data line between PCH and SPI flash device.  **SPI0 1 load topology:**  R1 is required 33Ω±5% for 1.8V, 62Ω±5% for 3.3V.  **SPI0 2 load topology:**  R1 is required 33Ω±5% for 1.8V, 56Ω±5% for 3.3V.  R2 is required 5Ω for 1.8V and 3.3V.  It is an optional to have R2 on the channel. It can be removed to reduce BOM cost.  **SPI0 3 load topology:**  R1 is required 15Ω±10% for 1.8V, 33Ω±5% for 3.3V.  R2 is required 10Ω for 1.8V and 3.3V. It is an optional to have R2 on the channel. It can be removed to reduce BOM cost.  **SPI0 1 load topology with EC Isolation FET Flash Sharing:**  R1 is required 33Ω±5% for 1.8V, 33Ω±5% for 3.3V.  **SPI0 2 load topology with EC Isolation FET Flash Sharing:**  R1 is required 33Ω±5% for 1.8V, 56Ω±5% for 3.3V.  **SPI0 3 load topology with EC Isolation FET Flash Sharing:**  R1 is required 15Ω±10% for 1.8V, 33Ω±5% for 3.3V.  **SPI0 1 load topology with EC Wired-OR Flash Sharing:**  R1 is required 0Ω placeholder for 1.8V and  15Ω for 3.3V.  R2 is required 50Ω for 1.8V and 50Ω for 3.3V.  R3 is required 33Ω for 1.8V and 50Ω for 3.3V.  **SPI0 2 load topology with EC Wired-OR Flash Sharing (2 flash):**  R1 is required 0Ω placeholder for 1.8V and 0Ω for 3.3V. For 3.3V.  R2 is required 50Ω for 1.8V and 100Ω for 3.3V.  R3 is required 15Ω for 1.8V and 15Ω for 3.3V.  R4 is required 15Ω for 1.8V and 15Ω for 3.3V.  **SPI0 2 load topology with EC Wired-OR Flash Sharing (1 flash and 1 TPM):**  R1 is required 0Ω placeholder for 1.8V and  0Ω for 3.3V.  R2 is required 50Ω for 1.8V and 100Ω for 3.3V. To be placed on SPI0\_CLK, SPI0\_MISO and SPI0\_MOSI.  R2 is required 50Ω for 1.8V and 50Ω for 3.3V. To be placed on SPI0\_IO\_2 and SPI0\_IO\_3. If TPM use this signal, R2 value shall follow MISO and MOSI recommendation.  R3 is required 15Ω for 1.8V and 15Ω for 3.3V. To be placed on SPI0\_CLK, SPI0\_MISO and SPI0\_MOSI.  R3 is required 33Ω for 1.8V and 50Ω for 3.3V. To be placed on SPI0\_IO\_2 and SPI0\_IO\_3. If TPM use this signal, R3 value shall follow MISO and MOSI recommendation.  R4 is required 15Ω for 1.8V and 15Ω for 3.3V. To be placed on SPI0\_CLK, SPI0\_MISO and SPI0\_MOSI. If TPM use SPI0\_IO\_2 and SPI0\_IO\_3, R4 value shall follow MISO and MOSI recommendation  **SPI0 3 load topology with EC Wired-OR Flash Sharing:**  R1 is required 0Ω placeholder for 1.8V and  0Ω for 3.3V. To be placed on SPI0\_CLK, SPI0\_MISO, SPI0\_MOSI, SPI0\_IO\_2 and SPI0\_IO\_3  R2 is required 15Ω for 1.8V and 100Ω for 3.3V. To be placed on SPI0\_CLK, SPI0\_MISO and SPI0\_MOSI.  R2 is required 50Ω for 1.8V and 50Ω for 3.3V. To be placed on SPI0\_IO\_2 and SPI0\_IO\_3. If TPM use this signal, R2 value shall follow MISO and MOSI recommendation  R3 is required 15Ω for 1.8V and 15Ω for 3.3V. To be placed on SPI0\_CLK, SPI0\_MISO and SPI0\_MOSI  R3 is required 15Ω for 1.8V and 15Ω for 3.3V . To be placed on SPI0\_IO\_2 and SPI0\_IO\_3. If TPM use this signal, R3 value shall follow MISO and MOSI recommendation  R4 is required 15Ω for 1.8V and 15Ω for 3.3V. To be placed on SPI0\_CLK, SPI0\_MISO and SPI0\_MOSI  R4 is required 15Ω for 1.8V and 15Ω for 3.3V for 3.3V. To be placed on SPI0\_IO\_2 and SPI0\_IO\_3. If TPM use this signal, R3 value shall follow MISO and MOSI recommendation  R5 is required 15Ω for 1.8V and 15Ω for 3.3V. To be placed on SPI0\_CLK, SPI0\_MISO and SPI0\_MOSI. If TPM use SPI0\_IO\_2 and SPI0\_IO\_3, R5 value shall follow MISO and MOSI recommendation. |
|  |

## Touch Host Controller (THC) Interface

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Pin Name** | **System Pull-up/ Pull-down** | **Series Termination Resistor** | **Notes** | **** |
| THC0\_SPI1\_CLK |  | 33 Ohm | Series Resistor R1 should be;  TGL-UP3/Y: 33Ω for 1.8V |  |
| THC0\_SPI1\_IO0 |  | 33 Ohm | Series Resistor R1 should be; TGL-UP3/Y: 33Ω for 1.8V |  |
| THC0\_SPI1\_IO1 |  | 33 Ohm | Series Resistor R1 should be; TGL-UP3/Y: 33Ω for 1.8V |  |
| THC0\_SPI1\_IO2 |  | 33 Ohm | Series Resistor R1 should be; TGL-UP3/Y: 33Ω for 1.8V |  |
| THC0\_SPI1\_IO3 |  | 33 Ohm | Series Resistor R1 should be; TGL-UP3/Y: 33Ω for 1.8V |  |
| THC0\_SPI1\_CS# |  |  | No series-resistor required. |  |
| THC0\_SPI1\_RST# |  |  | No series-resistor required. |  |
| THC0\_SPI1\_INT# |  |  | No series-resistor required. |  |
| THC1\_SPI2\_CLK |  | 33 Ohm | Series Resistor R1 should be; TGL-UP3/Y: 33Ω for 1.8V |  |
| THC1\_SPI2\_IO0 |  | 33 Ohm | Series Resistor R1 should be; TGL-UP3/Y: 33Ω for 1.8V |  |
| THC1\_SPI2\_IO1 |  | 33 Ohm | Series Resistor R1 should be; TGL-UP3/Y: 33Ω for 1.8V |  |
| THC1\_SPI2\_IO2 |  | 33 Ohm | Series Resistor R1 should be; TGL-UP3/Y: 33Ω for 1.8V |  |
| THC1\_SPI2\_IO3 |  | 33 Ohm | Series Resistor R1 should be; TGL-UP3/Y: 33Ω for 1.8V |  |
| THC1\_SPI2\_CS# |  |  | No series-resistor required. |  |
| THC1\_SPI2\_RST# |  |  | No series-resistor required. |  |
| THC1\_SPI2\_INT# |  |  | No series-resistor required. |  |

## 

## eSPI

Table 23. eSPI Interface Checklist

|  |  |  |
| --- | --- | --- |
| **Pin Name** | **System Implementation** | **Notes** |
| ESPI\_IO[3:0] | 15 Ohm series resistor | The 15 Ohm resistors are for place holders and can be removed after verifying signal integrity on the signals.  Place the resistors as close as possible to the PCH. |
| ESPI\_CLK | 50 Ohm series resistor | 50 Ohm series resistor is required. Place the resistor as close as possible to the PCH. |
| ESPI\_RESET# ESPI\_CS# | No resistor needed. | Direct point to point connection.  **Note** : It is recommended to add a PD resistor of 75K on ESPI\_RESET for PCH glitch free implementation. |

## I2C

Table 24. I2C Interface Checklist

|  |  |  |  |
| --- | --- | --- | --- |
| **Pin Name** | **System Pull-up/ Pull-down** | **Schematics Notes** |  |
| I2C[5:0]\_SCL I2C[5:0]\_SDA | May require Internal Pull- down resistor and current assist along with External pull-up resistor. | The external pull-up resistor and current assist value depends on the speed supported and total bus capacitance. Refer I2C chapter in the Platform Design Guide for details. |  |

## SMBus Interface and System Management

Table 25. SMBus Interface and System Management Interface Checklist

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Pin Name** | **System Pull-up/ Pull-down** | | **Schematics Notes** | | |  |
| SMBCLK, SMBDATA | Note: Multiple options for the pull-up / pull-down resistor and current assist strengths are provided for a particular Total bus capacitance. Choose an optimal value for the system based on the design considerations like power dissipation, BoM cost.  Additional circuitry may be required to connect high and low powered sections. | | Value of external pull-up resistor, internal pull-down resistor and current assist is determined by load capacitance and bus speed. For PCI Express\* compliance, SMBus signals should be routed to either all or none of the PCI Express devices in a chassis.  If SMBus is connected to PCIe\*, it must be connected to all PCIe\* slots.  Refer SMBus Architecture and design consideration section in Tiger Lake U/Y Platform Design Guide. | | |  |
| SMBALERT# | External Pull-up resistor required. | |  | | |  |
| PMCALERT# | External Pull-up resistor required. | | In case Integrated USB-C is being used. | | |  |
| SML0ALERT# | External Pull-up resistor required | |  | | |  |
| SML1ALERT# | External Pull-up resistor required | |  | | |  |
| SML[0:1]DATA SML[0:1]CLK | Multiple options for the pull-up /pull- down resistor and current assist strengths are provided for a particular Total bus capacitance. Choose an optimal value for the system based on the design considerations like power dissipation, BoM cost.  Additional circuitry may be required to connect high and low powered sections. | | External Pull-up, internal Pull-down value and current assist is determined by bus characteristics. | | |  |
| Intel® ME Requirements—For all platforms that do not have an RJ45 LAN connector (No on-board LAN) and have DRAM soldered down to the motherboard | | | | | | |
| HW Requirement | | Expected Configuration | | Verified (Y/N) | Issues/ Next Steps | |
| Implement Test Points for the 3 SMbus pins (Data, clk and GND). | | Test points are expected on PCB to hook external SMbus sniffer to the SMbus and to sniff the PDA tool output data.  Refer to SMBus Architecture and design consideration section in Tiger Lake U/Y Platform Design Guide. | |  |  | |

## Controller Link

Table 26. Controller Link Checklist

|  |  |  |
| --- | --- | --- |
| **Pin Name** | **Schematics Notes** |  |
| CL\_RST# | Controller Link reset that connects to a Wireless LAN Device supporting Intel® Active Management Technology. |  |
| CL\_CLK | Bi-directional clock that connects to a Wireless LAN Device supporting Intel® Active Management Technology |  |
| CL\_DATA | Bi-directional data that connects to a Wireless LAN Device supporting Intel® Active Management Technology. |  |

## UART

Table 27. UART Interface Checklist

|  |  |  |  |
| --- | --- | --- | --- |
| **Pin Name** | **System Pull-up/ Pull-down** | **Schematics Notes** |  |
| UART\_RXD[2:0] UART\_TXD[2:0] UART\_RTS[2:0] UART\_CTS[2:0] |  | If the interface is used, pull-up is the device dependent and not mandatory.  If the interface is not used, the signals can be used as GPIO. If GPIO functionality is also not used, the signals can be left as no- connect. |  |

## GPIO

Refer to the Tiger Lake External Design Specification (EDS) for details on GPIO multiplex and straps.

For Glitch implementation details on required PCH GPIO signals, refer to Tiger Lake Platform Design Guide.

All unused GPIO pins that default to GPIO functionality do not need termination. For unused GPIO pins that default to a native function, termination on the pins depend on the termination requirement of the native function. Refer to the Tiger Lake External Design Specification (EDS) (# 576591) for details on GPIO multiplex information.

## CNVi Interface Signals

Refer to the below document link for the latest CNVi schematic checklist (# [575882](https://cdrdv2.intel.com/v1/dl/getContent/575882)).

## Intel® ME

Table 28. ME-EC Interaction for All Platforms Supporting Intel® CSE Corporate and Consumer Designs

|  |  |  |  |
| --- | --- | --- | --- |
| **Hardware Requirement** | **Expected Configuration** | **Verified (Y/N)** | **Comments** |
| ME-EC Interaction for All Platforms Supporting Intel® CSE  Corporate and Consumer Designs | | | |
| Intel® ME-EC: Intel® ME-EC connections according to latest revision of Intel® ME-EC Interaction Specification. Please refer to “Converged Security and Manageability Engine (CSME) and Embedded Controller (EC) Interaction”, # 626375 for more details on implementation. | | | |
| SLP\_S3# | Optional for platforms with M3 support.  Required for platforms without M3 support. If SLP\_A# is routed from PCH to EC, then SLP\_S3# can be optional from Intel® ME-EC perspective. |  |  |
| SLP\_A# | Required for platforms with M3 support.  SLP\_A# should be routed from the PCH to the EC. SLP\_A# asserted low informs the EC when Intel® ME is in an CMOff state. Depending on the platform, this pin may be used to control power to various devices that are part of the ME sub-system in the platform. |  |  |
| ACPRESENT | Required for systems with and without M3.  The ACPRESENT pin is used by EC for indicating the current power source of the system to Intel® ME. When asserted, it indicates that the platform is connected to an AC source. |  |  |
| SUSPWRDNACK | This signal is called GPP\_A2/ESPI\_IO2/SUSWARN#\_SUSPWRDNACK in the PCH documentation.  This pin asserts low when the PCH is planning to enter the Deep Sx power state and remove Primary power (by using SLP\_SUS#). The EC / motherboard controlling logic must observe the edges on this pin, preparing for the Primary well power loss on the falling edge and preparing for Primary well related activities (which are host / Intel® ME wakes and runtime events) on the rising edge. SUSACK# must be driven to match SUSWARN# once the above preparation is complete. SUSACK# should be asserted within a minimal amount of time from SUSWARN# assertion as no wake events are supported if SUSWARN# is asserted but SUSACK# is not asserted yet. Platforms supporting Deep Sx, but not wishing to participate in the handshake during wake and Deep Sx entry may tie SUSACK# to SUSWARN#. SUSWARN# is multiplexed with SUSPWRDNACK since SUSPWRDNACK is not needed in Deep Sx supported platforms. |  |  |
| SLP\_SUS# | Deep Sx Indication: When asserted (driven low), this signal indicates PCH is in Deep Sx state where internal Sus power is shut off for enhanced power saving. When de-asserted (driven high), this signal indicates the exit from Deep Sx state and Sus power can be applied to PCH. For non-Deep Sx, this pin also needs to use to turn on the VCCPRIM\_1P8 VR. This pin cannot be left unconnected.  ***Note:*** This pin is in the DSW power well. |  |  |
| SUSACK# | Active low signal. It is an input to the PCH (driven by EC) and is involved in Deep Sx entry and exit flows. For more information about SUSACK#.  For platforms that do not support DeepSx mode, this signal can be left unconnected. |  |  |

Table 29 Hardware and EC firmware Requirements Checklist - All Platforms Supporting Intel® Active Management Technology (Intel® AMT) Corporate Designs only

|  |  |  |  |
| --- | --- | --- | --- |
| Hardware Requirement | Expected Configuration | Verified (Y/N) | Comments |
| ME-EC Interaction for All Platforms Supporting Intel® Active Management Technology (Intel® AMT) Corporate Designs only | | | |
| Intel® ME-EC: Intel® ME-EC connections according to latest revision of Intel® ME-EC Interaction Specification. Please refer to “Converged Security and Manageability Engine (CSME) and Embedded Controller (EC) Interaction”, CCL# 626375 for more details on implementation. | | | |
| SLP\_A# | Required if platform supports M3, otherwise optional. |  |  |
| CL\_CLK | Controller Link Clock: Bi-directional clock that connects to a Wireless LAN Device supporting Intel® Active Management Technology. For Controller Link design guidelines, refer to “Tiger Lake UP3/UP4 Platform Design Guide", ”PCH IOs" chapter, CCL# 607872 for more details. |  |  |
| CL\_DATA | Controller Link Data: Bi-directional data that connects to a Wireless LAN Device supporting Intel® Active Management Technology. For Controller Link design guidelines, refer to “Tiger Lake UP3/UP4 Platform Design Guide", ”PCH IOs" chapter, CCL# 607872 for more details. |  |  |
| CL\_RST# | Controller Link Reset: controller link reset pin that connects to a Wireless LAN Device supporting Intel® Active Management Technology. For Controller Link design guidelines, refer to “Tiger Lake UP3/UP4 Platform Design Guide", ”PCH IOs" chapter, CCL# 607872 for more details. |  |  |
| SLP\_LAN# | SLP\_LAN# is asserted when power can be shut off to the PHY device(s). SLP\_LAN# will always be de-asserted in S0 and anytime SLP\_A# is de-asserted.  \*\*Power to LAN while it is powered must not be interrupted by either hardware or EC firmware on any of events (which include warm reset, power-cycle reset). |  |  |
| SLP\_WLAN# | SLP\_WLAN# is asserted when power can be shut off to the external wireless LAN device. SLP\_WLAN# will always be de-asserted in S0.  \*\*To support WLAN out-of-band in both S0 and Sx/AC states, the WLAN device must always be powered and connected to primary 3.3V rail.  \*\*Power to WLAN, while it is powered must not be interrupted by either hardware or EC firmware on any of events (which include warm reset, power-cycle reset). |  |  |
| TLS Confidentiality | Customer are expected to enable the strap. |  |  |

Table 30 Hardware and EC firmware Requirements Checklist - All Platforms Supporting Intel® CSE Corporate and Consumer Designs

|  |  |  |  |
| --- | --- | --- | --- |
| Hardware Requirement | Expected Configuration | Verified (Y/N) | Comments |
| Platform Design Recommendation for All Platforms Supporting Intel® CSE  Corporate and Consumer Designs | | | |
| Design Guide provides motherboard implementation recommendations for the Tiger Lake UP3 and UP4 platforms, based on the Tiger Lake processor. Please refer to “Tiger Lake UP3/UP4 Platform Design Guide", CCL# 607872 or “Tiger Lake Platform Controller Hub External Design Specification (EDS)”, CCL# TBD for more details. | | | |
| SPI Write-Protect Pin | Must be pulled up to one of the following rails: A rail enabled by of SLP\_LAN# or SLP\_A#. |  |  |
| SPI Flash Connectivity | SPI flash must be directly connected to the PCH for Intel® ME. Intel recommends having a Flash socket for validation, but it is not required for production releases. |  |  |
| DnX Pin Strap | GPPC\_E\_22 Muxing of DNX\_FORCE\_RELOAD. Refer to "Tiger Lake Platform Controller Hub External Design Specification (EDS) – Volume 1 of 2" for more details. |  |  |
| SPI Flash Descriptor Security Override | GPP\_R2 / HDA\_SDO / I2S0\_TXD signal is used for Flash Descriptor Security Override (which is also known as Intel® ME Debug Mode). This signal input should be tied to a jumper which connects to power through an external pull-up (1 KΩ ±5%) only. When this signal is asserted, the Flash Security gets overridden for ease of image programming. Please refer to “Tiger Lake Platform Controller Hub External Design Specification (EDS)” document for further details. |  |  |
| Power Sequence | Customers should ensure their platform follow the timing constraints spelled out in the “Platform Power Sequencing Specification” chapter in PDG document. |  |  |
| Intel® PCH XDP Debug port | Connect the PCH JTAG signals directly to PCH XDP debug port connector as described in the “Platform Debug and Test Hooks” chapter in PDG document. |  |  |
| Intel® APS Connectors | Customers are expected to follow the PDG and implement one of the two Intel® APS connectors as recommended in Intel® APS section in PDG document |  |  |

## Intel® ISS

This section provides schematics, PCB Layout and System checklists for the Tiger Lake IISS design to support in the design review and provide additional filter to catch design errors. Intel recommends that customer will make the best design according to the design guidelines provided, will run over the following checklist and will consult with Intel Application Engineers if there is any violation to the IISS Design Guidelines.

When to Use this Checklist?

* Schematics: To be performed after schematics is done before PCB Layout design.
* PCB Layout: To be performed after chassis and PCB layout are done before Gerber.
* System: To be performed after system is fully assembled and powered.

1. Be noticed on your early designs. It is strongly recommended to reserve pads of series resistor and stuff with 0 Ohm resistors on ISH\_I2Cx and ISH\_GPx. Designers could separate sensor components onto ISH\_I2C0 and ISH\_I2C1. By doing this, it can keep flexibility of circuits if an adjustment is needed on your PCB.
2. For the Magnetometer, a special white paper was composed for supporting Magnetometer integration. Refer to Mobile Computer Platform, Magnetometer Design Integration Technical White Paper (# 535305).

### Schematics Design Checklists

All labels may be prefixed with ISH\_ if needed to differentiate them from other system schematic labels.

This section is used to record the actual sensors that the designer selected to use on his/her design. Based on the sensor used, the following tables should be filled by the designer with the specific selected sensors data.

|  |  |  |
| --- | --- | --- |
| **General** | **Verified (Y/N)** | **Comments** |
| Did you read, understood and followed all your sensors manufacturers design guidelines? |  |  |
| Did you add Layout instructions to the schematics, for the layout designer to implement, such as keep-out zones for sensors, as mentioned in “System Debug” in PDG? |  |  |
| Specify your Form-factor type (Clamshell, 360-Clamshell or ...) |  |  |

|  |  |  |
| --- | --- | --- |
| **Accelerometer Sensor** | **Verified (Y/N)** | **Comments** |
| Sensor Part number? |  |  |
| I2C bus the Sensor is connected to? (ISH\_I2C0, ISH\_I2C1 or ISH\_I2C2) |  |  |
| I2C address on the i2C bus? |  |  |
| Is there an option to use alternative I2C Address? If so, what is the alternative I2C Address? |  |  |
| Interrupt available? |  |  |
| Interrupt polarity? (Active high or active low) |  |  |
| Interrupt I/O buffer type? (Totem Pole or Open drain) |  |  |
| Is the same interrupt line shared with other component(s)? (ISH FW does not support it.) |  |  |
| VDD voltage? (1.8V or 3.3V) |  |  |
| VDDIO voltage? (1.8V or 3.3V) |  |  |
| Is a level-shifter placed between the sensor and ISH\_I2Cx? |  |  |
| Is a level-shifter placed between the sensor and ISH\_GPx? |  |  |

|  |  |  |
| --- | --- | --- |
| **The 2nd Accelerometer Sensor** | **Verified (Y/N)** | **Comments** |
| Sensor Part number? |  |  |
| I2C bus the Sensor is connected to? (ISH\_I2C0, ISH\_I2C1 or ISH\_I2C2) |  |  |
| I2C address on the i2C bus? |  |  |
| Is there an option to use alternative I2C Address? If so, what is the alternative I2C Address? |  |  |
| Interrupt available? |  |  |
| Interrupt polarity? (Active high or active low) |  |  |
| Interrupt I/O buffer type? (Totem Pole or Open drain) |  |  |
| Is the same interrupt line shared with other component(s)? (ISH FW does not support it.) |  |  |
| VDD voltage? (1.8 V or 3.3 V) |  |  |
| VDDIO voltage? (1.8 V or 3.3 V) |  |  |
| Is a level-shifter placed between the sensor and ISH\_I2Cx? |  |  |
| Is a level-shifter placed between the sensor and ISH\_GPx? |  |  |

|  |  |  |
| --- | --- | --- |
| **Gyroscope Sensor** | **Verified (Y/N)** | **Comments** |
| Sensor Part number? |  |  |
| I2C bus the Sensor is connected to? (ISH\_I2C0, ISH\_I2C1 or ISH\_I2C2) |  |  |
| I2C address on the i2C bus? |  |  |
| Is there an option to use alternative I2C Address? If so, what is the alternative I2C Address? |  |  |
| VDD voltage? (1.8V or 3.3V) |  |  |
| VDDIO voltage? (1.8V or 3.3V) |  |  |
| Is a level-shifter placed between the sensor and ISH\_I2Cx? |  |  |

|  |  |  |
| --- | --- | --- |
| **Magnetometer Sensor** | **Verified (Y/N)** | **Comments** |
| Sensor Part number? |  |  |
| I2C bus the Sensor is connected to? (ISH\_I2C0, ISH\_I2C1 or ISH\_I2C2) |  |  |
| I2C address on the i2C bus? |  |  |
| Is there an option to use alternative I2C Address? If so, what is the alternative I2C Address? |  |  |
| VDD voltage? (1.8 V or 3.3 V) |  |  |
| VDDIO voltage? (1.8 V or 3.3 V) |  |  |
| Is a level-shifter placed between the sensor and ISH\_I2Cx? |  |  |

|  |  |  |
| --- | --- | --- |
| **Ambient Light Sensor (ALS)** | **Verified (Y/N)** | **Comments** |
| Sensor Part number? |  |  |
| I2C bus the Sensor is connected to? (ISH\_I2C0, ISH\_I2C1 or ISH\_I2C2) |  |  |
| I2C address on the i2C bus? |  |  |
| Is there an option to use alternative I2C Address? If so, what is the alternative I2C Address? |  |  |
| Interrupt available? |  |  |
| Interrupt polarity? (Active high or active low) |  |  |
| Interrupt I/O buffer type? (Totem Pole or Open drain) |  |  |
| Is the same interrupt line shared with other component(s)? (ISH FW does not support it.) |  |  |
| VDD voltage? (1.8 V or 3.3 V) |  |  |
| VDDIO voltage? (1.8 V or 3.3 V) |  |  |
| Is a level-shifter placed between the sensor and ISH\_I2Cx? |  |  |
| Is a level-shifter placed between the sensor and ISH\_GPx? |  |  |

|  |  |  |
| --- | --- | --- |
| **Pressure Sensor** | **Verified (Y/N)** | **Comments** |
| Sensor Part number? |  |  |
| I2C bus the Sensor is connected to? (ISH\_I2C0, ISH\_I2C1 or ISH\_I2C2) |  |  |
| I2C address on the i2C bus? |  |  |
| Is there an option to use alternative I2C Address? If so, what is the alternative I2C Address? |  |  |
| Interrupt available? |  |  |
| Interrupt polarity? (Active high or active low) |  |  |
| Interrupt I/O buffer type? (Totem Pole or Open drain) |  |  |
| Is the same interrupt line shared with other component(s)? (ISH FW does not support it.) |  |  |
| VDD voltage? (1.8V or 3.3V) |  |  |
| VDDIO voltage? (1.8V or 3.3V) |  |  |
| Is a level-shifter placed between the sensor and ISH\_I2Cx? |  |  |
| Is a level-shifter placed between the sensor and ISH\_GPx? |  |  |

### BOM Checklist

|  |  |  |
| --- | --- | --- |
| **Intel Sensor Solution BOM** | **Verified (Y/N)** | **Comments** |
| Are all the Intel® ISH managed sensors supported in Intel POR BOM? Specify them if they are not in the BOM. |  |  |
| Did you make sure your vendor will provide support to you with Intel® ISH FDK if your selected sensor(s) is/are not in Intel POR BOM? |  |  |
| Did you make sure there is no conflict with I2C address on the same ISH I2C bus? |  |  |
| Did you review the I2C design and make sure it conforms to the I2C Design Guidelines in PDG? |  |  |

### Sensors Debug Connector Checklist

|  |  |  |
| --- | --- | --- |
| **Sensors Debug Connector** | **Verified (Y/N)** | **Comments** |
| Was one of the two proposed debug connectors implemented in this design? Refer to “Sensors Debug Hooks” in PDG. |  |  |

### FW Debug Connector Checklist

|  |  |  |
| --- | --- | --- |
| **FW Debug Connector** | **Verified (Y/N)** | **Comments** |
| Was the XDP or the Primary CMC Debug Solution implemented? Refer to “Platform Debug and Test Hooks” for more detail in PDG. |  |  |

### Power Rails Checklist

|  |  |  |
| --- | --- | --- |
| **Power Rails** | **Verified (Y/N)** | **Comments** |
| Did you check that all sensors connected to power rails with correct voltages? |  |  |
| Did you check that all sensors connected to ISH I2C interface with correct voltage level? (Is a voltage level shifter needed?) |  |  |
| Did you check that all sensors connected to ISH GPIO interface with correct voltage level? (Is a voltage level shifter needed?) |  |  |

### Sensors I2C/Interrupt/GPIO Checklist

|  |  |  |
| --- | --- | --- |
| **Sensors I2C/Interrupt/GPIO** | **Verified (Y/N)** | **Comments** |
| Did you make sure there is no conflict with I2C address on the same ISH I2C bus? |  |  |
| Did you correctly set the Address Selection pin on each of the sensors, to be accessible on its selected address? |  |  |
| Did you check that all the sensors that are located on the same I2C bus operate at the selected frequency? |  |  |
| Did you review the I2C design and make sure it conforms to the I2C Design Guidelines which includes “Electrical Characteristics” in PDG? |  |  |
| Did you review the GPIO design and make sure it conforms to the GPIO Design Guidelines which includes “Electrical Characteristics” in PDG? |  |  |

### PCB Layout and System Design Checklists

The PCB Layout and System design checklist is documented to provide our customer’s PCB Layout and System design assistance to verify that the customer will produce the best accuracy reading sensor data by followed the IISS system design guidelines. We recommend that customer will make the best design according to the design guidelines provided and will consult with Intel Application Engineer if this PCB Layout and System check results violates IISS design guidelines. Not following design guidelines will result in a system with **less** than best performance possible.

When using sensors package that contains more than one sensor, this package should conform to the design guidelines for all sensors in the same package. Therefore, all sensors checklists should be used for that package.

When to Use this Checklist?

Use this checklist as follows:

* After board's components are placed (according to the design guidelines) before PCB Layout starts.
* After PCB Layout was done before closing the PCB design for gerber files.
* During and after system's chassis design for LID magnets, hinges, speakers, microphone, fan, cooling system, hot spots location, wireless charger and digitizers. Some of them may impact sensors accuracy.
* On any PCB layout change.
* On any chassis re-design.

1. For the Magnetometer, a special white paper was composed for supporting Magnetometer integration. Refer to Mobile Computer Platform, Magnetometer Design Integration Technical White Paper (# 535305).

Sources to this PCB Layout and System Checklist:

* Schematics checklist.
* Sensor vendors documentation.
* Accumulated knowledge and experience gathered by Intel Application Engineers.

#### General Mechanical Sensor Placement and Assembly Checklist

|  |  |  |
| --- | --- | --- |
| **Items** | **Verified (Y/N)** | **Comments** |
| PCB Layout | | |
| Did you read, understand and follow all the layout and design rules requirements from your sensor manufacturers? |  |  |
| Did you read and understand the “Magnetometer Design Integration - Technical White Paper”, #535305? |  |  |
| **Did you make sure that the sensor placement was the first step when outlining a new PCB layout and system Chassis? You need to plan accordingly, accommodating both board and system level.** |  |  |
| In the Chassis level, did you place sensors at an interference-free location in the system for **all its usage models**? |  |  |
| Did you avoid placing the sensors in a long and narrow region of PCB? From our learning shows that doing this can warp and cause sensor package stress which may cause drift. |  |  |
| Did you avoid placing the sensor near a connector and screw hole? Doing it will cause unsymmetrical stress coming from PCB deformation when a screw is inserted will cause drift. |  |  |
| Did you avoid placing the sensor in a region of PCB that can warp? Doing it might cause sensor package stress which may cause shift. |  |  |
| System Layout | | |
| Were all sensors placed 2 or 3 cm away from any hot devices? This helps to avoid large temperature gradient. |  |  |
| Did you make sure that sensors are not placed in a region of PCB that can warp? It can cause package stress which may cause shift. |  |  |
| Did you make sure that sensors are not placed near a connector or screw hole? It can cause an unsymmetrical stress coming from PCB deformation and may cause drift. |  |  |
| For a 360-degree system, checklist defined in the PCB Layout above should be run for all usage models, meaning Lid is in 0-degree, 180-degree and 360-degree etc. |  |  |
| For a Detachable (2-in-1) system, checklist defined in the PCB Layout above should be run for all usage models, meaning Tablet mode, Laptop mode where Lid is at 0-degree (Lid closed), 90-degree and the maximum. |  |  |

#### Accelerometer

|  |  |  |
| --- | --- | --- |
| **Items** | **Verified (Y/N)** | **Comments** |
| PCB Layout | | |
| Is the Accelerometer mounted securely, so it cannot move independently? |  |  |
| System Layout | | |
| Are the Accelerometer X, Y and Z axes orientated as described in PDG? |  |  |
| Is the Accelerometer placed in a stable position, isolated from any vibration, including transmitted vibration, air pressure change vibration, etc.? |  |  |
| Is the Accelerometer place at least 30 mm away from audio speakers, fans, and haptic vibration motors? |  |  |

#### Gyroscope

|  |  |  |
| --- | --- | --- |
| **Items** | **Verified (Y/N)** | **Comments** |
| PCB Layout | | |
| Is the Gyroscope mounted securely, so it cannot move independently? |  |  |
| System Layout | | |
| Are the Gyroscope X, Y and Z axes orientated as described in PDG? |  |  |
| Is the Gyroscope placed in a stable position, isolated from any vibration, including transmitted vibration, air pressure change vibration, etc.? |  |  |
| Is the Gyroscope place at least 30 mm away from audio speakers, fans, and haptic vibration motors? |  |  |

#### Magnetometer

|  |  |  |
| --- | --- | --- |
| **Items** | **Verified (Y/N)** | **Comments** |
| PCB Layout | | |
| **Have you read and understood the Mobile Computer Platform, Magnetometer Design Integration Technical White Paper (# 535305)?** |  |  |
| **The Magnetometer can easily become an issue if the design guidelines are not followed. Did you follow all of the Design Guidelines provided in PDG?** |  |  |
| **Was the magnetometer placement the first step when outlining a new PCB layout?** |  |  |
| **Was the magnetometer placed at least 40 mm away from any rare earth magnets (Hard Iron such as speaker magnets, LID magnets, fan, Hall Effect magnet etc.)?** |  |  |
| **Was the Magnetometer placed at least 30 mm away from any large/thick (structural) ferrous metals, the components which includes the magnet of a hard disk, digitizer, and any components with the magnetism of 100 Gauss?** |  |  |
| Was the Magnetometer placed at least 10 mm away from the components which include microphone, vibration motor, magnetic switch, transformer, camera module, beeper, battery, SAW filter, antenna, power amplifier, choke, LCD rear case and any components with the magnetism of 5 Gauss? |  |  |
| Was the Magnetometer placed at least 5 mm away from the components which include Memory/SIM card socket, USB connector, other connectors, screw, nut, spring, EMI shielding part, and any components with the magneto conductive material (Iron, Cobalt, Nickel)? |  |  |
| Was the Magnetometer placed at least 2 mm away from the surrounding resistor and capacitor? This, since nickel plating is usually present on solder end caps of surface mount components? |  |  |
| Was the Magnetometer placed at least 10 mm away from the power trace (including power plane) on all the PCB layers, components on both PCB sides or out of the board with the variable current higher than 10 mA? |  |  |
| Was the Magnetometer placed at least 20 mm away from the power trace (including power plane) on all the PCB layers, components on both PCB sides or out of the board with the variable current higher than 100 mA? |  |  |
| Was the Magnetometer placed at least 25 mm away from the power trace (including power plane) on all the PCB layers, components on both PCB sides or out of the board with the variable current higher than 200 mA? |  |  |
| **Is there any power or ground plane under or nearby the Magnetometer? (There should be none)** |  |  |
| Make sure the Magnetometer is not covered with any material that can block the static magnetic field from the earth. |  |  |
| System Layout | | |
| **Did you make sure that the LCD screen back shell, shield (for RF, BT…), mechanical part (key, screw, connector) do not contain ferromagnetism material (Fe, Co, Ni)? (correct answer is no)** |  |  |
| **Did you perform the same test as in the PCB layout when the PCB is inside the final chassis, when system is powered?** |  |  |
| **All the above tests must be checked in all usage models, such as a 360-degree system, interference for the Lid located Magnetometer should be checked with Lid in 0-degree, 180-degree and 360-degree.** |  |  |

#### Ambient Light Sensor – ALS

|  |  |  |
| --- | --- | --- |
| **Items** | **Verified (Y/N)** | **Comments** |
| System Layout | | |
| Is the ALS placed in the lid or display module, close to the camera (if present) and facing the user? This will allow effective control of screen brightness based on ambient light. |  |  |
| Are the view angle and the lens meeting the spec of the ALS? |  |  |
| Is the glass or plastic covering material consistent across the units of the same SKU/Model? |  |  |
| Is the aperture wide enough to detect light without significant attenuation when the light source is at an angle to the device or from a diffused source? |  |  |
| Are the glass/cover and the sensor aligned? (a misalignment would mask out some of the light and produce unexpected readings from the ALS) |  |  |
| If optical film or ink coating are applied to hide the ALS optical cavity, is the filter designed to allow at least 80% of visible wavelength light to pass? |  |  |

#### Pressure Sensor

|  |  |  |
| --- | --- | --- |
| **Items** | **Verified (Y/N)** | **Comments** |
| System Layout | | |
| Is the clearance above the metal lid less than 0.1mm? |  |  |
| Is the sensor located in a section where appropriate venting exists? |  |  |
| Is the sensor located in an area where liquids may come into direct contact with the device? |  |  |
| Is there a direct light heating the sensor? Direct light can influence the accuracy of the measurement (photo-current of silicon). |  |  |
| Is the sensor located near a source of fast air pressure variation, such as fans, speaker etc.? |  |  |
| Is the sensor located near a source of fast heating parts with gradients higher than 3°C/sec? |  |  |
| Is the PCB area below the sensor defined as keep-out area? |  |  |

#### Debug Connector (10051922-1810elf)

|  |  |  |
| --- | --- | --- |
| **Items** | **Verified (Y/N)** | **Comments** |
| PCB Layout | | |
| Was the connector implemented on the PCB? |  |  |
| System Layout | | |
| Was the connector placed in an area where accessing it does not require opening the chassis? |  |  |

## Electromagnetic Compatibility

Table 31. Component Placement Review Checklist

|  |  |  |
| --- | --- | --- |
| **Item #** | **Description** | **Y/N** |
| 1 | Clock synthesizers, crystals, oscillators, microprocessor chips and other VLSI packages have been placed in the center of the board, away from board edges, I/O connectors, plane splits and other board mounted connectors to minimize radiation from the board. |  |
| 2 | Components using the same clock have been placed close to each other and the clock source to minimize clock trace lengths. |  |
| 3 | Filter components have been placed adjacent to the pin they are filtering on I/O connectors. |  |
| 4 | For non-differential clocks, provisions have been made for series termination of clock traces at the source to minimize ringing. |  |
| 5 | Ensure that the following interfaces have common mode chokes installed:   * HDMI * USB 2.0 * USB 3.2 * DP |  |

Table 32. General Routing Review Checklist

|  |  |  |
| --- | --- | --- |
| **Item #** | **Description** | **Y/N** |
| 1 | Board stack-up designed to ensure that all clocks and high-speed (> 1 MHz) traces are routed in layers adjacent to power or ground planes. |  |
| 2 | Power planes have been recessed from the edge of the board. |  |
| 3 | Clock traces have been laid out first and kept as short as possible, consistent with the need for matched clock trace lengths in the clock nets. |  |
| 4 | Clock and High-Speed traces do not change layers and do not cross breaks in power or ground planes. Stitching capacitors must be used in areas were reference breaks are unavoidable. |  |
| 5 | Clock and High-Speed traces have been kept away from board edges and traces leading to connectors (internal or external connections). |  |
| 6 | Clock and High-Speed differential traces have been laid out to minimize length, consistent with the need for matched trace lengths to minimize signal skew. |  |
| 7 | Do not route traces under clock generating circuits or other large high-speed devices. |  |
| 8 | Ground pads with the same footprint as the part have been provided on the component side of the board away from oscillators or clocks. These ground pads are tied to the ground plane(s) of the board with multiple vias. |  |
| 9 | Provisions have been made for bonding the board ground system to the chassis at multiple points. The best locations are at connectors and noise sources (clocks, microprocessors, etc.). |  |
| 10 | Provisions have been made for grounding the heat plate or heat sink on the microprocessor to the board ground structure. |  |

Table 33. I/O Routing Review Checklist

|  |  |  |
| --- | --- | --- |
| **Item #** | **Description** | **Y/N** |
| 1 | All I/O connectors have been provided with a low impedance bond to chassis for their shield structure. |  |
| 2 | All non-ground nets routed externally, should have a filter present. |  |
| 3 | I/O connector traces route to ESD protection before any other device. |  |

Table 34. Decoupling / Filtering Review Checklist

|  |  |  |
| --- | --- | --- |
| **Item #** | **Description** | **Y/N** |
| 1 | SMT bypass capacitors are connected directly to power and ground planes with minimum trace length between the part and via. |  |
| 2 | Bypass capacitor values have been selected to insure minimum impedance in the frequency range(s) of interest. |  |
| 3 | Filter capacitors (line to ground) have been provided a low impedance path to chassis as close to the capacitor as possible. |  |

Table 35. ESD Checklist

|  |  |  |
| --- | --- | --- |
| **HDAItem #** | **Description** | **Y/N** |
| 1 | All hot-plug interfaces, should have ESD protection present (HDMI, USB2, USB3.2, Audio, SIM Card Interface, Docking Connector and SD Card). |  |
| 2 | Implement a ground shape continuous along the board edge, outside of any traces. Keep the gap between the ground shape and other shapes or traces at least 0.5mm. The minimum shape neck width is 0.75mm. The minimum fill area should be 20% of the connector footprint under each connector. |  |
| 3 | Add stitching vias throughout the length of the ground shape, no more than 2.5 mm apart, close to the board's edge (connector holes can be considered stitching vias). |  |

## Power Sequencing

Table 36. Power Sequencing Schematic Checklist

|  |  |  |  |
| --- | --- | --- | --- |
| **Power rail/ Signal Name** | **System Pull-up/ Pull-down** | **Schematics Notes** | **** |
| VCCRTC |  | RTC Supply. RTC Power can be supplied either from coin cell (tPCH04a) or through a LDO (tPCH04b – non coin cell timing requirement) – Nominal Value – 3.3V |  |
| SRTCRST#/  RTCRST# | RC delay in the range of 18-25 ms. | RTC Reset.  RC time delay for SRTCRST# should be the same as RC delay for RTCRST#.  RTCRST# and SRTCRST# cannot be shorted together. |  |
| VCCDSW\_3P3 |  | DSW Power Rail. Nominal Value – 3.3V.  This rail can be shorted to VCCPRIM\_3P3 in case of Non-DSX designs |  |
| DSW\_PWROK |  | Connect Power Good (PG) of VCCDSW VR to DSW\_PWROK with delay of 10 ms or more.  Normally, PG are open drain. Hence needed PU. |  |
| SLP\_SUS# |  | SLP\_SUS# will be driven high by SoC. This should be connected to VCCPRIM\_3P3 VR EN in case of DSx designs.  Can be connected to VCCRIM\_1P8 VR EN in case of Non-DSx designs.  Also, add SLP\_SUS# to AND gate which is generating RSMRST#. Refer to DSx/Non-DSx Architecture Block Diagram. |  |
| VCCPRIM\_3P3 |  | PRIMARY Well 3.3V Power Rail.  Short this rail with VCCDSW\_3P3 in case of Non-DSx designs  SLP\_SUS# should enable VCCPRIM\_3P3 VR in case of DSx designs |  |
| VCCPRIM\_1P8 |  | PRIMARY Well 1.8V Power Rail.  SLP\_SUS# should enable VCCPRIM\_1P8 VR in case of Non-DSx designs  PRIM\_3P3 VR PG should enable VCCPRIM\_1P8 VR for DSx designs |  |
| VCCIN\_AUX |  | PCH Core Rail  Nominal Voltage – 1.8V  Connect VID0 and VID1 from VCCIN\_AUX\_VID0/1 with PU resistors to VCCPRIM\_3P3 or VCCPRIM\_1P8 depending on GPP voltage  PRIM\_1P8 VR PG should enable VCCIN\_AUX VR |  |
| VNN\_BYPASS |  | VNN Power Rail  Nominal Voltage – 1.05V  Can be left unconnected if Integrated FIVR to be used  Else, can be powered externally with VNN VR and should be enabled by VCCIN\_AUX PG  Connect SLP\_S3# and VNN\_CTRL signal from SoC to VIDs of VR. Please refer to Power Delivery section of PDG for more details on VNN EXT VR Voltage Configurations |  |
| VCC\_1P05\_EXT BYPASS |  | EXT Power Rail  Nominal Voltage – 1.05V  Can be left unconnected if Integrated FIVR to be used  Else, can be powered externally with VNN VR and should be enabled by VNN\_BYPASS VR PG  Connect V1P05\_CTRL signal from SoC to VID of the VR. Please refer to Power Delivery section of PDG for more details on V1P05 EXT VR Voltage Configurations |  |
| RSMRST# |  | Input to PCH  RSMRST# can be generated by the platform VCC\_1P05\_EXT\_BYPASS VR PG logically AND’d with DSW VR PG with delay, SLP\_SUS#  In case of FIVR to be used, VCCIN\_AUX PG can be used to generate RSMRST# logically AND’d with DSW VR PG with delay, SLP\_SUS# |  |
| PLTRST# |  | Connect to reset of all devices that need a reset (SIO, IDE, TPM, PCI Express\* slot, PCI Express down device and so forth) on the motherboard.  Required a pull down resistor or capacitor site |  |
| VCCST\_OVERRIDE |  | If TCSS Wake-up is enabled, this signal will be driven High in S5, S4 and S3 states. The Voltage level of this signal is 1.05V. Please level translate the signal to 3.3V while connecting this to OR gate of VCC 3.3V. |  |
| VCCSTPWRGD\_TCSS |  | Short this signal with VCCST\_OVERRIDE. Refer to Asynchronous sideband signal for more information |  |
| VCCST\_PWRGD |  | Indication that the VCCSTG\VCCST\VDDQ power supplies are stable and within specification. Input to SoC. Voltage level of the signal is 1.05V. Level translator is required if the operating voltage of derived logic is not 1.05V. |  |
| VCCST |  | VCCST power rail can be enabled by OR Gate logic of SLP\_S3#, VCCST\_OVERRIDE (level translated) and XDP\_PRESENT (optional – for debug). VCC1P05\_OUT\_FET power rail from SoC can be used to derive VCCST. |  |
| VCCSTG |  | VCCSTG power rail can be enabled by OR Gate logic of CPU\_C10\_GATE#, VCCST\_OVERRIDE (level translated) and XDP\_PRESENT (optional – for debug). VCC1P05\_OUT\_FET power rail from SoC can be used to derive VCCSTG. |  |
| THRMTRIP# | 1 kohm to 10 kohm pull-up to VCCST. | A low value pull-up is OK since THRMTRIP# only goes low to shut down. In normal operation this signal is high. |  |
| SLP\_S3#  SLP\_S4#  SLP\_SUS#  SLP\_A#  SLP\_WLAN#  SLP\_LAN# |  | Driven by PCH after RSMRST# de-assertion  100K (3.3V) / 75K (1.8V) PD resistor required for Glitch free implementation during boot |  |
| SLP\_S0# |  | Please refer to PCH Glitch Free Implementation chapter for Pullup requirement - Signal driven by the PCH. |  |
| SLP\_A# |  | Can be left as NC when Intel® Active Management Technology (Intel® AMT) is not supported on the platform or there are no devices on the platform that is tied to Intel® AMT. |  |
| SLP\_LAN# |  | If using integrated LAN, connect signal to control PHY subsystem power. If not using integrated LAN, signal may be left as NC. |  |
| SLP\_WLAN# |  | SoftStrap selectable with default SLP\_WLAN#. Signal driven by the PCH. If using WLAN, connect signal to control WLAN subsystem power. If not using WLAN, signal may be left as NC. |  |
| PCH\_PWROK | 10 kohm to 100 kohm pull-down to GND. | When asserted, PWROK is an indication to the PCH that all of its core power rails have been stable. The platform may drive asynchronously PCH\_PWROK high any time after it has met all the required sequencing timings called out in the sequencing section of this Design Guide. When PWROK is negated, the PCH asserts PLTRST#  IMVP\_VR\_READY AND’d with IMVP\_VR\_ON generate PCH\_PWROK  NOTE: If this signal is driven from an open drain source/ buffer (active low) the pull-up resistor should be sufficient.  NOTE: The pulldown is not needed if the source of this signal can guarantee this signal is in proper state for G3 through S0 |  |
| SYS\_PWROK | 10kohm to 100 kohm pull- down to GND | System Power OK: This generic power good input to the PCH is driven and utilized in a platform-specific manner. While PWROK always indicates that the CORE well of the PCH is stable, SYS\_PWROK is used to inform the PCH that power is stable to some other system component(s) and the system is ready to start the exit from reset. The particular component(s) associated with SYS\_PWROK can vary across platform types supported by the same generation of PCH. Depending on the platform, the PCH may expect (and wait) for SYS\_PWROK at different stages of the boot flow before continuing.  **NOTES:**   * 1. SYS\_PWROK should be asserted with or after PCHPWROK and VR\_PWRGD for the core VR. This needed to ensure a safe platform design which meets the timing requirements for this signal. Refer to the latest platform power sequence specification for details.   2. If this signal is driven from an open drain source/ buffer (active low) the pull-up resistor should be sufficient.   **NOTE:** The pulldown is not needed if the source of this signal can guarantee this signal is in proper state for G3 through S0. And if PCH\_PWORK and SYS\_PWROK are tied together only on common pulldown is needed. |  |
| PWRBTN# |  | The power button signal (PWRBTN#) on PCH can be connected directly to the power button on the system.  This signal has an internal pull-up resistor and has an internal 16 ms de-bounce on the input. This signal is in the DSW well.  Drive this PWRBTN# low for at least 20 ms to be recognized as Power Button Press.  **NOTE:** If the power button is powered in G3 state, when the PCH is unpowered, the platform must buffer the signal from the hard power button before it connects to the PCH PWRBTN# signal pin. The buffered version of PWRBTN# signal should be open drain and pulled up to the PCH 3.3DSW. This is required to prevent leakage into the PCH in G3 states and when PCH is unpowered. |  |
| LANPHYPC | No external resistors required. | LANPHYPC should be connected to LAN\_DISABLE\_N on the PHY. PCH will drive LANPHYPC low to put the PHY into a low power state when functionality is not needed.  Intel CRBs may have an empty pull-up resistor for testing purpose. |  |
| WAKE# | 1 kohm pull-up to VCCDSW\_3p3. | The pull-up is required even if PCIe\* interface is not used on the platform.  **NOTE:** Ensure that WAKE# signal Trise (Maximum) is <100 ns. Refer to PCI Express\* Mini- Card Electromechanical 2.0 Specification and PCI Express\* Card Electromechanical 2.0 Specification for details. |  |
| SLP\_S5# |  | Need resistor pull down or capacitor site for glitch free implementation  Driven High when systems enter to S4 or higher states. Low in S5 and all other lower states |  |
| EXT\_PWR\_GATE#/EXT\_PWR\_GATE2# |  | These signals from SoC to be used as EN signals for VCCMPHYGT\_1P05 and VCCPRIM\_GATED\_1P05 in UP4 Platform only. These gating circuits are no longer mandatory to implement. However, existing designs with gates can continue with them. This is applicable only for UP4 sku only. |  |
| BATLOW#/GPD0 | 10 kΩ to 100 kΩ pull-up to DSW well. | Pull-up required even if not implemented. |  |
| ACPRESENT/ GPD1 | 100 kΩ pull-up to DSW rail. | Point-to-point connection between PCH and EC. To indicate that system is powered by AC. This is a required signal for platforms with or without M3 support. A lower value pull- down is OK here on this signal because it only draws power when the brick is present (no impact to battery life).  Refer to Tiger Lake PCH-LP Platform Controller Hub External Design Specification (EDS) for details. |  |
| SUSWARN#/ SUSPWRDNACK/ |  | Will be eSPI Virtual Wire and no hard signal. |  |
| CPU\_C10\_GATE# | Pulldown for glitch free - 100KΩ for 3.3V/75KΩ for 1.8V | Connect to VR EN pin of VCCSTG to turn OFF the VR in C10 state. This is used as power saving option in C10 and S0ix. Please refer to PCH Glitch Free Implementation chapter for Pulldown resistor requirement and for more details |  |

## Platform Debug and Test Hooks Checklist

|  |  |  |
| --- | --- | --- |
| **Signal Connection Recommendation** | **Verified (Y/N)** | **Comments** |
| Refer your Intel Field Representative if additional information on manufacturing boundary scan testing is needed |  |  |
| **Open Chassis Debug Methodology** 1. Follow the table 252 Debug Port Signal Mapping for MIPI60 Debug implementation  2. Follow the section 12.1.2 Intel Small Form Factor Debug Connector for 20 Pin SFF Debug Implementation  Please refer the limitations mentioned w.r.t 20 pin Intel Small Form Factor debug connector and mitigation plan suggested in this section in PDG. |  |  |
| **Processor and PCH JTAG Signal Connections** 1. Follow section 12.1.3 as mentioned in PDG for proper termination of 2. Processor and PCH JTAG Signal Connector for Intel DCI Implementation |  |  |
| **Intel DCI.OOB Configuration Supporting USB3 Type A** 1. No re-timer to be used 2. Signals to be routed from PCH USB3  3. For designs that do not have a type A or with type A but with re-drivers, make sure one of the unused type A ports are routed to test points/header. |  |  |
| **Additional Test Points** In order to help Intel with further debug, please route all the TP, RSVD\_TP and GPD11/ LANPHYPC/DSWLDO\_MON as test points |  |  |
| **Depopulation Guidelines for Debug Port** 1. Debug port real estate and pads remain in place - if they need to be populated for future. 2. TGL UP3/UP4 has adequate internal bias resistance on JTAG, PROC\_PREQ# and PROC\_PRDY# signals to keep the devices in an idle state without the external pull up resistors 3. It is acceptable to replace the standard resistor values with any resistor value between 51Ohm to 3k ohm to reduce bill-of-material items when the debug is no longer needed. Processor BPM#[3:0] signals can be left floated when not used for debug. 5. Processor CFG[19:0] and PCH Chipset test interfaces might have dual purpose usage. 6. From Debug port perspective, external components (resistor, jumper, or FET switch) between debug connector and chipset test interfaces can be removed when debug is no longer needed. 7. However there might be a need to keep the strap resistor and external components in place for the non debug usage of the interfaces. |  |  |

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